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TEST METHODS AND CUSTOM HARDWARE FOR FUNCTIONAL TESTING OF A HIGH SPEED GaAs DRAM

by
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TEST METHODS AND CUSTOM HARDWARE FOR FUNCTIONAL TESTING OF A HIGH SPEED GaAs DRAM

by

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Submitted in partial fulfillment
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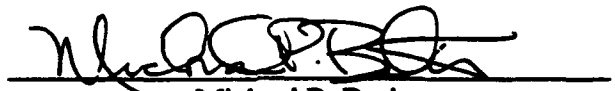
Author: 
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ABSTRACT

The goal of this project is to produce a digital circuit operating near a frequency of 250 MHz to test a new experimental Gallium Arsenide (GaAs) Dynamic Random Access Memory (DRAM). This thesis presents the design of the digital circuit using "off-the-shelf" Emitter Coupled Logic (ECL) and the design of a six layer printed circuit test fixture. The use of ECL is illustrated including general design rules, high speed design considerations, and basic transmission line theory. Finally, the design is laid out and simulated using commercially available Computer Aided Design (CAD) and Computer Aided Manufacturing (CAM) tools. Examples and shortcomings of schematic capture, logic simulation, PCB design, and autorouting are discussed as applicable to fabrication of the final product.

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I. INTRODUCTION

Dynamic read/write memory (DRAM) is a basic component of the modern computer system. Since the arrival of the "age of the personal computer", dynamic RAM is commonly discussed on the business pages of major newspapers of the world. An announcement by a major manufacturer may be front page news or an item for the broadcast media. Perhaps the only other product of technology to receive such wide attention is the announcement of a new microprocessor.

In terms of technical advancement, DRAM has seen major developments in capacity over the past ten years, yet very little advancement in terms of speed or change in architecture. DRAM architecture and performance have been "good enough" and "cheap enough" until the arrival of the new classes of personal computers and workstations that have been announced in the recent past.

A. CURRENT INITIATIVES

A discussion of DRAM architecture is beyond the scope of this paper and is included only to present basic design and access rates. The components discussed here [Ref. 1] are considered the more favorable products and areas of research. They are all silicon-based. All four examples are considered ideal candidates to mate with the Intel Pentium, Motorola PowerPC, and DEC Alpha processors to support major increases in clock rates expected to surpass 150 MHz by 1995.

- Cache DRAM (CDRAM)-- the mating of a standard DRAM (rated at 70 nsec) with an onboard static memory cache.
- Enhanced DRAM (EDRAM)-- similar to CDRAM with the exception that a smaller static memory cache is integrated to a fast 35 nsec DRAM .

- Synchronous DRAM (SDRAM)-- synchronizing the DRAM with the system clock that enables the memory to operate at CPU clock speeds. Current initiatives are rated at 100 MHz.
- RAMBUS DRAM (RDRAM)-- a totally new DRAM architecture that promises bus rates of 450 MBps as opposed to 33 MBps that is typical for current asynchronous DRAM.

It should be noted that there have been no major developments or announcements in dynamic RAM other than in density for several years. The driving force for these new products is shown in Figure 1-1 [Ref. 1], presented on the following page showing and predicting the growth of microprocessor clock speed as opposed to DRAM operating specifications. Until a new high speed DRAM is available, designers must continue to utilize static RAM (SRAM) caches and bus interfaces to maintain throughput to the computer's central processing unit (CPU).

B. THE NPS GALLIUM ARSENIDE DRAM

The subject of this thesis is related to a Gallium Arsenide Dynamic Read/Write Memory (GaAs DRAM) developed at the Naval Postgraduate School (NPS) and fabricated by Vitesse Semiconductor. The basic DRAM cell design using gallium arsenide was a product of previous research [Ref. 2], and the actual chip design was done in MAGIC and simulated in HSPICE [Ref. 3] at a speed of 250 MHz.

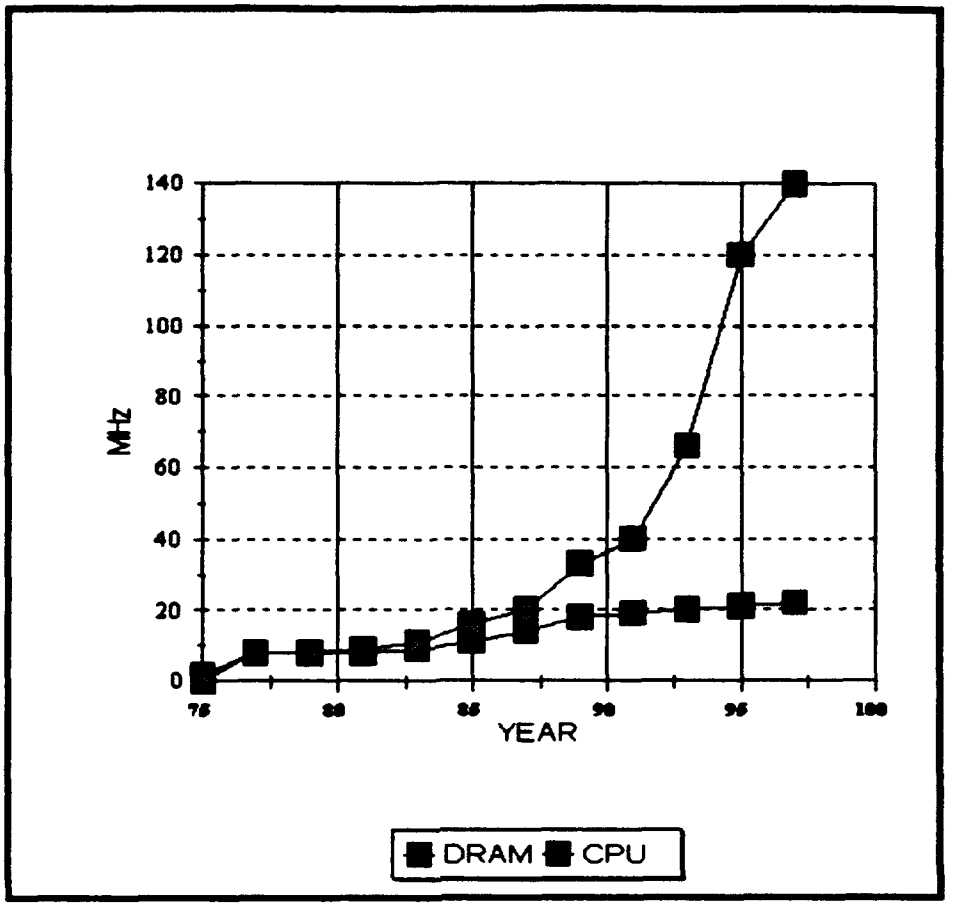


Figure 1-1 DRAM vs. CPU Speed Performance

The NPS GaAs DRAM completed the fabrication and packaging process in August 1993 and is now available for testing. However, the testing can be addressed in a number of ways. From past research literature on testing memories, a common approach is to hook the component to a signal generator and oscilloscope, test basic function, and measure performance characteristics in terms of access time and noise margins. It is generally a "we made it, it works, and it is this fast" approach.

The testing plan for the GaAs DRAM is different. The operational characteristics and speed parameters need to be tested in a more controlled environment. Speeds of over 200 MHz are desired, and study of DRAM reaction to signals simulating actual

computer operation are the goal. Considering that commercially available (and affordable) DRAM test equipment operates in the 20 MHz range (expensive testers are obtainable to speeds neighboring 80 MHz) it is necessary to build a custom digital test circuit and printed circuit board to read and write data to the DRAM under test.

C. GENERAL DESIGN PARAMETERS

The DRAM test circuit will be presented in detail during the following discussion. A listing of major design attributes is presented to provide an overview of the project.

- The GaAs DRAM is a 32-bit memory consisting of eight address locations by four bits of information. The only external control line used in this project is the data ready (DRDY) signal provided by the DRAM.
- The DRAM interfaces to external logic by means of Emitter Coupled Logic (ECL) technology. The manufacturer of the ECL components is National Semiconductor.
- Due to the edge rates and speed, all lines are required to be terminated following transmission line interconnect techniques. The standard used for ECL termination is 50 ohm termination to -2.0 volts.
- The function of the test circuit is to write data to a given address and then read it back out of the RAM. The design will allow the DRAM to have eight addresses of data written and then read back out. The intent is to do this at the highest speed possible to test the DRAM's speed parameters.
- To build a circuit board of reasonable size, the use of Surface Mount Technology (SMT) is required. The size factor is directly related to the speed to be achieved due to interconnect propagation.
- To achieve the clock speed necessary to adequately test the DRAM, the fixture must contain dedicated signal planes for high speed logic. These impedance controlled signal planes must be bounded on the top and bottom by either power or ground planes to reduce crosstalk and reflections.

All of the above considerations are carried out by Computer Aided Design (CAD) software to design the circuit and build a Printed Circuit Board (PCB). Schematic netlists will be transferred to PCB design software to draw the board layout. Additionally, each logic section will be transferred to an ECL capable logic simulator to check the function, speed, and timing requirements of each functional block.

D. APPLICATIONS

The use of GaAs in commercial applications has dramatically increased with the need for speed. Manufacturing density and yield has improved, as have the necessary design tools. The number of engineers who have been trained in the technology is growing. GaAs teamed with ECL has been used in supercomputers for a number of years. ECL has incorporated commercial improvements by manufacturers after a decade of dormancy. There is real interest in high speed digital design ranging from components involved to the printed circuit boards they are mounted on.

Research and fabrication of a DRAM that is capable of three nanosecond access without onboard cache, complex bus architecture, or separate microprocessor to direct memory traffic has real application. The silicon-based examples that were the subject of research papers less than ten years ago are now being commercially manufactured. However, they still do not provide the speed and performance demanded by the new microprocessors. Continued research will provide GaAs memories of higher density, simple architecture, and the needed speed. Pursuing improvements in manufacturing may make GaAs competitive in the future.

II. DRAM TEST METHODS AND LOGIC DESIGN

The purpose of this chapter will be to describe the GaAs DRAM interface and outline the ECL logic used in the test circuit. Each area is accompanied by a functional schematic, a description, and applicable timing information to support the design.

Timing analysis was performed on SUSIE-CAD [Ref. 4], a WINDOWS© based schematic capture and logic simulation program. As the SUSIE libraries do not support the new National Semiconductor 300 Series ECL products, timing data is a scaled approximation of the F100K ECL series. The differences are minor and are discussed in the text if necessary.

A. THE GaAs DRAM PHYSICAL LAYOUT

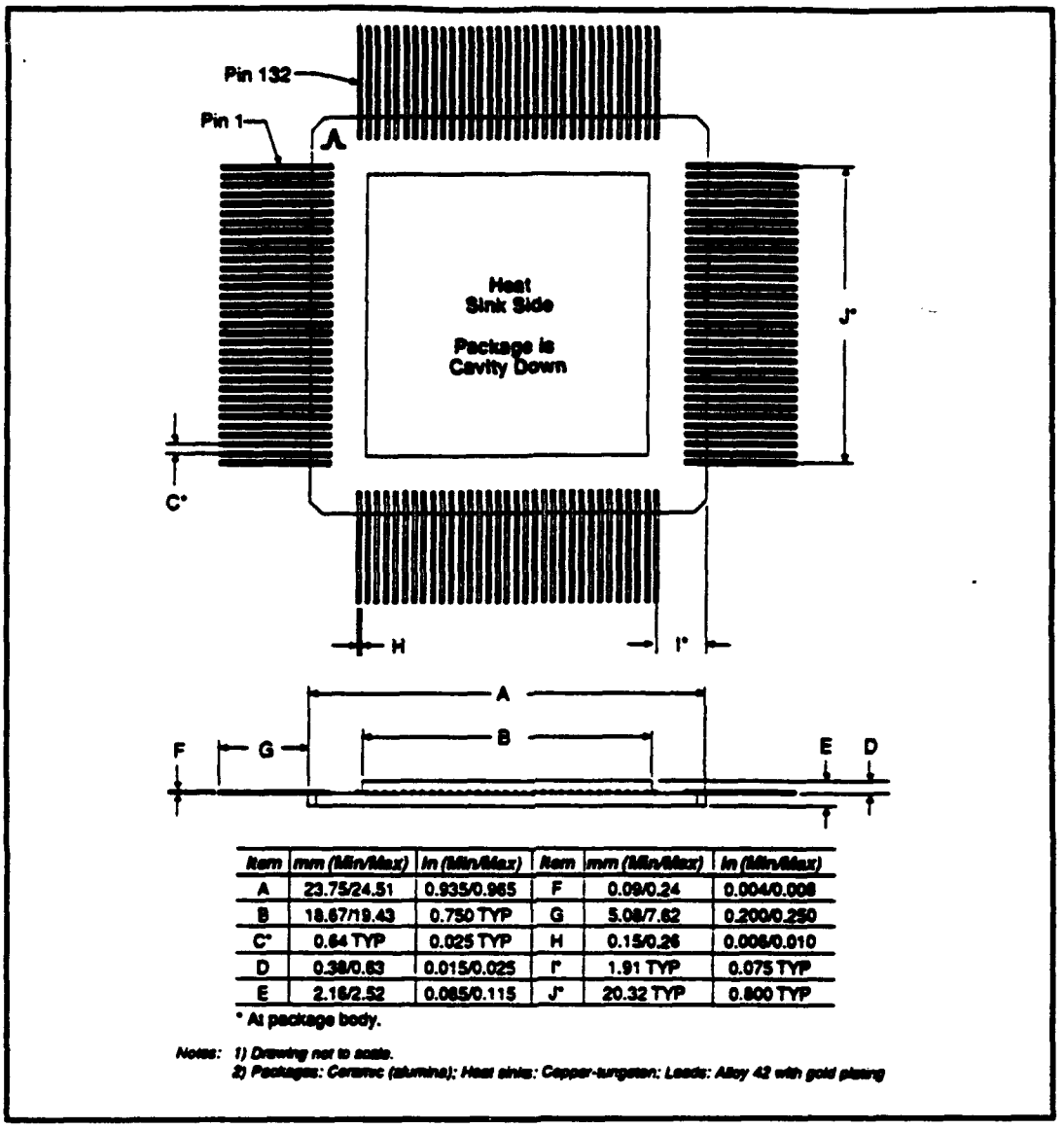
Throughout the course of the project the size and pinout of the GaAs DRAM were unknown. Initially due for delivery in May 1993, the size of the die resulted in a much larger package than expected. The planned 52-pin flat-pak doubled, and finally resulted in a 132-pin Leaded Ceramic Chip Carrier (LDCC). Final pinout for the circuit was not available until mid-August. The DRAM package consists of 132 pins in a surface mount (SMT) case measuring less than one inch square and .2 inches high with pin categories shown below. Table 2-1 shows the pin assignments and Figure 2-1 is the LDCC (approximately 2X actual size).

- 12 inputs (3 address / 4 data / clock / READ / WRITE / data strobe (DAS) / REFRESH)
- 6 outputs (4 data / memory busy (MBSY) / data ready (DRDY))
- 12 power (VDD to -2.0V)
- 34 ground (GND)
- 1 substrate (SUB) connected to most negative system voltage

- 1 level shifting power supply (VSS)
- 1 ECL receiver pad reference voltage (RVREF)
- 2 DRAM cell reference array voltages (VREFD/VREFB)
- 63 unconnected pins (NC)

TABLE 2-1 PIN ASSIGNMENTS FOR THE LDCC

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	NC	34	GND	67	NC	100	GND
2	RVREF	35	INCLK(I)	68	NC	101	NC
3	GND	36	NC	69	GND	102	NC
4	GND	37	GND	70	GND	103	GND
5	-2.0V	38	D0(I)	71	-2.0V	104	VSS
6	NC	39	NC	72	NC	105	NC
7	WRITE(I)	40	D1(I)	73	NC	106	VREFB
8	READ(I)	41	GND	74	-2.0V	107	GND
9	NC	42	GND	75	NC	108	GND
10	NC	43	-2.0V	76	NC	109	-2.0V
11	REFRESH(I)	44	NC	77	D0(O)	110	NC
12	NC	45	D2(I)	78	NC	111	VREFD
13	NC	46	NC	79	NC	112	NC
14	A2(I)	47	GND	80	D1(O)	113	GND
15	NC	48	D3(I)	81	NC	114	NC
16	GND	49	NC	82	GND	115	NC
17	SUB	50	A0(I)	83	-2.0V	116	NC
18	NC	51	NC	84	NC	117	NC
19	NC	52	GND	85	D2(O)	118	GND
20	GND	53	DAS(I)	86	NC	119	DRDY(O)
21	NC	54	NC	87	NC	120	NC
22	NC	55	NC	88	D3(O)	121	MBSY(O)
23	GND	56	GND	89	NC	122	GND
24	NC	57	GND	90	NC	123	GND
25	NC	58	-2.0V	91	NC	124	-2.0V
26	GND	59	NC	92	NC	125	NC
27	NC	60	NC	93	NC	126	GND
28	GND	61	NC	94	GND	127	NC
29	-2.0V	62	GND	95	-2.0V	128	GND
30	GND	63	NC	96	GND	129	-2.0V
31	NC	64	NC	97	NC	130	NC
32	A1(I)	65	GND	98	NC	131	GND
33	NC	66	NC	99	NC	132	-2.0V



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	23.75/24.51	0.935/0.965	F	0.09/0.24	0.004/0.009
B	18.67/19.43	0.750 TYP	G	5.08/7.62	0.200/0.250
C*	0.64 TYP	0.025 TYP	H	0.15/0.26	0.006/0.010
D	0.38/0.63	0.015/0.025	I*	1.91 TYP	0.075 TYP
E	2.16/2.52	0.085/0.115	J*	20.32 TYP	0.800 TYP

* At package body.

Notes: 1) Drawing not to scale.
2) Package: Ceramic (alumina); Heat sink: Copper-tungsten; Leads: Alloy 42 with gold plating

Figure 2-1 Vitesse Databook Diagram of 132-pin LDCC

All DRAM signals are converted between gallium arsenide technology and ECL voltage levels at the I/O pads. The GaAs DRAM can be considered an integrated ECL memory circuit for all intensive purposes. The requirements for the signal interfaces were derived from graphs and documentation produced by previous research [Ref. 3]. Table 2-2 is a summary of the internal signals and interface parameters.

TABLE 2-2 GaAs DRAM INTERNAL/INTERFACE SIGNAL PARAMETERS

DESIGNATION	USE	INTERNAL VOLTAGE LEVELS	DEPENDENCIES & INFO
A0:A2	Address Inputs	LOW 0.0 to 0.4 V HIGH 1 to 1.1 V	Δ Clock @ nominal 250 MHz-Variable for test
D0:D3	Data Inputs	LOW 0.0 to 0.4 V HIGH 1 to 1.1 V	Δ Clock @ nominal 250 MHz-Variable for test
DAS	Data Strobe	LOW 0.0 to 0.4 V HIGH 1 to 1.1 V	Negative edge strobes input data
INCLK	DRAM System Clock	0.0 TO 0.7 V 50% Duty Cycle	Variable for test purposes simulator clock @ 250MHz
VDD	Main Chip Positive Power Supply	-2.0 V	≅1.31 amps(simulated)
VSS	Negative Supply for Level Shift	-2.5 V	≅69 milliamp(simulated)
VR VREF	Receiver Pad Reference	.7 V	≅1.1 milliamp (simulated)
VREFD	Dummy Precharge Reference	.26 V	≅300 microamp (simulated)
VREFB	Bitline Precharge Reference	.7 V	≅5 milliamp (simulated)
READ	Read Command Signal	LOW .4 V HIGH 1.1 V	Test limits ≅ Access Time @ 3 nsec
WRITE	Write Command Signal	LOW .4 V HIGH 1.1 V	Test limits ≅ Access Time @ 3 nsec
REFRESH	Refresh Clock	LOW .4 V HIGH 1.1 V	25KHz 10% Duty Cycle Pulse Signal
D0:D3	Data Outputs	LOW 0.0 to 0.1 V HIGH .5 V	
MBSY	Memory Busy	LOW 0 V HIGH 1.1 V	Asserted on Read/Write or Refresh
DRDY	Data Ready	LOW 0 V HIGH 1.1 V	Asserted on Read/Write or Refresh

The only timing consideration is that the data must be valid and then strobed into the DRAM input registers by DAS during a WRITE operation. The strobe is activated by a negative edge. DAS specifics will be discussed later in the control section.

B. ECL LOGIC DESIGN FOR HIGH SPEED TESTING

The DRAM test circuit is composed of four sections. The register groups, control logic and manual clock, refresh counter, and drivers. Before introducing the sections, a generalized block diagram (Figure 2-2) is shown below with the four register groups (input data, output data, address, and READ/ WRITE). The control group uses the data ready (DRDY) signal from the DRAM to produce data strobe (DAS) and register shifting signals. Refresh provides a pulse to the DRAM for internal timing. Drivers provide static logic inputs. The Manual switch allows for all the above functions so that individual tests may be performed as necessary.

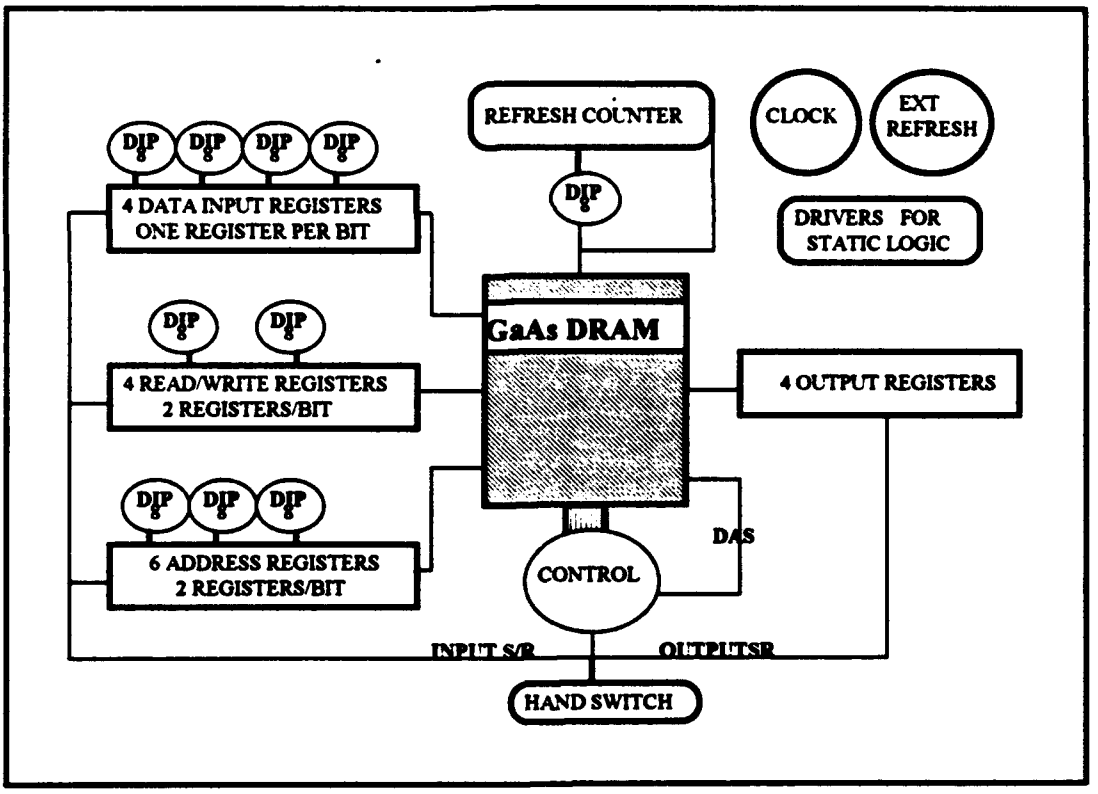


Figure 2-2 Generalized Block Diagram

1. The Refresh Counter

The purpose of the refresh counter is to pulse the DRAM at approximately three msec intervals to refresh the storage cells within the DRAM array. Operation is performed by five 4-bit National Semiconductor 100336A counters that divide the incoming system clock by 16^5 based on a 250 MHz clock coming onto the board. The outputs of the last counter are routed to a DIP switch that allows the pulse time base to be selected depending on the input test frequency. This allows some choice during testing of the refresh rate. An extra pad is available on the circuit board to route an external signal for refresh testing. This allows decoupling the refreshment logic from the design if needed. The time base selections are in Table 2-3 and the accompanying schematic is shown as Figure 2-3.

TABLE 2-3 REFRESH COUNTER TIMEBASE

CLOCK FREQUENCY (SYSCLOCK)	75 MHz	100 MHz	125 MHz	150 MHz	175 MHz	200 MHz	225 MHz	250 MHz
OUTPUT Q0 (in msec)	1.75	1.31	1.05	0.87	0.75	0.66	0.58	0.52
OUTPUT Q1 (in msec)	3.50	2.62	2.10	1.75	1.50	1.31	1.17	1.05
OUTPUT Q2 (in msec)	6.00	5.24	4.19	3.50	3.00	2.62	2.33	2.10
OUTPUT Q3 (in msec)	14.0	10.5	8.39	6.99	5.99	5.24	4.66	4.19

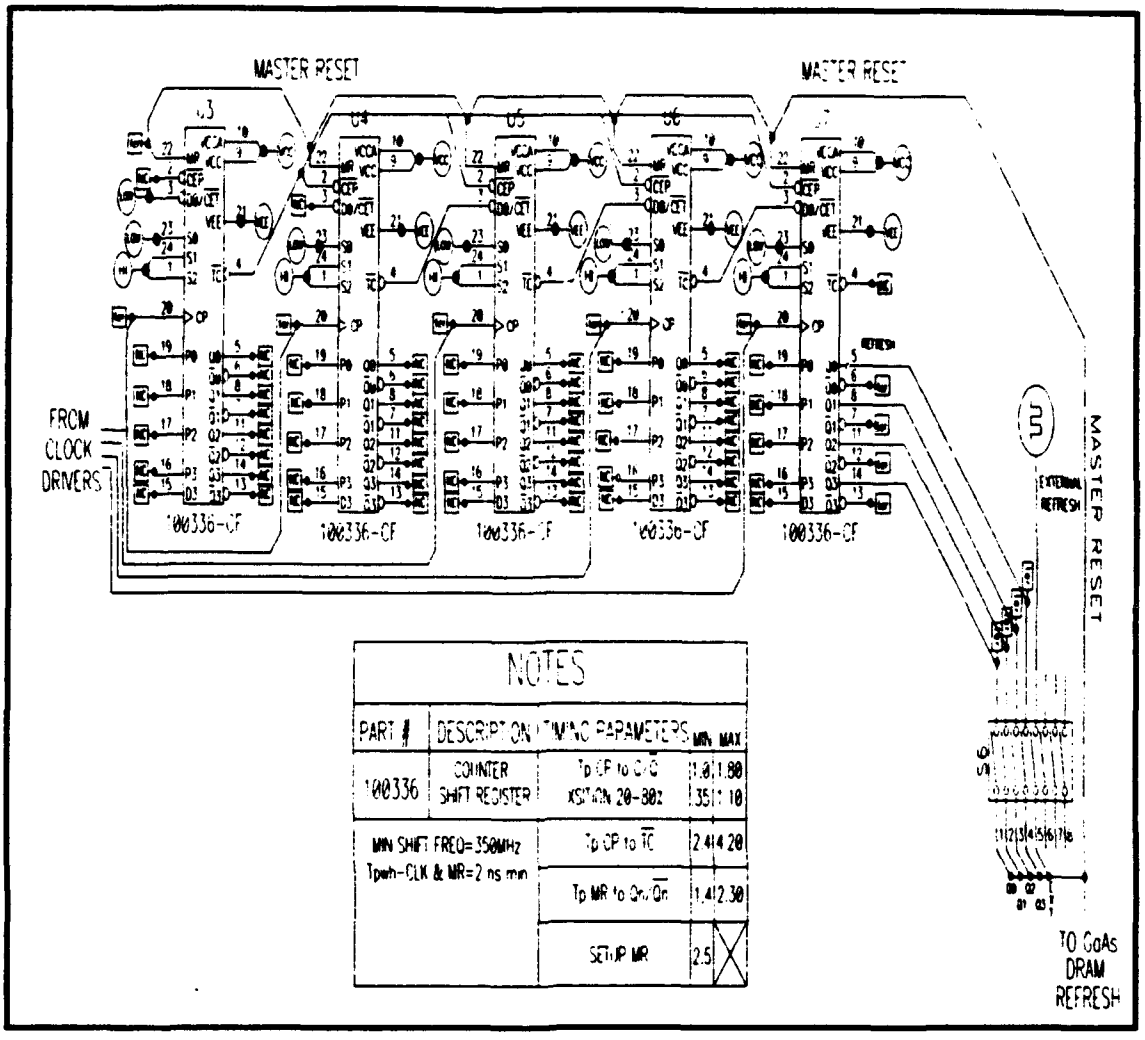


Figure 2-3 Refresh Counter

The circuit shown in Figure 2-3 is presented in all three data books used during research [Ref. 5, 6, 7]. The layout is known as a "fast counter" scheme that allows the terminal count signal (nTC) of the first counter (which goes LOW at 1111) to enable all following stages. The remaining counters are enabled by the nTC signal of the previous counter. This scheme reduces the delay to one count enable trickle (nCET) to nTC propagation delay plus one count enable pulse (nCEP) to clock pulse (CP) setup time. By using the typical timing characteristics of the National 1003XX series the

refresh counter should operate to 225 MHz. All register controls (S0/S1/S2) are static with the selected refresh pulse routed back to all master reset (MR) inputs to start a new counting cycle. The timing diagram for the count sequence is shown below in Figure 2-4 for the first two counters (due to space limitations). The design does not allow for initialization of the counters as all unconnected inputs are pulled low (ECL standard), and the SUSIE simulation allows for a "random" start sequence simulation that shows the counters should initialize on their own.

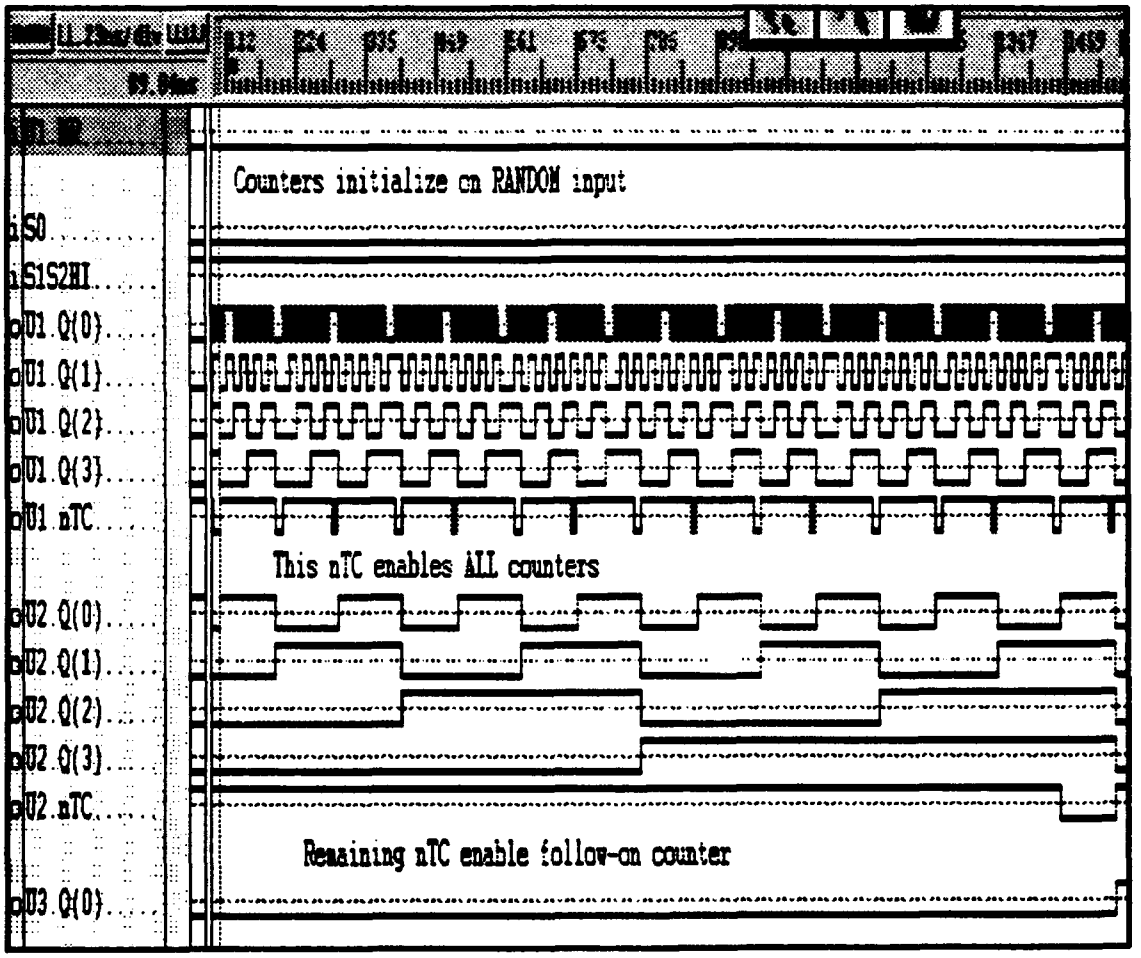


Figure 2-4 Refresh Count Sequence

Figure 2-5 shows the reset of the counters when they reach the desired refresh interval. Q0 is selected on the last counter (for example, from Table 2-3 would be 0.58 msec at 225 MHz). When Q0 goes high, it acts as the reset to all counters causing them to initialize and resume a new count sequence. The requirement for the master reset (MR) pulse is a minimum 2.0 nsec high pulse width and a release time of 2.5 nsec. Considering the following delays (1) CP to Q0, (2) line delay Q0 to all MR inputs, and (3) MR release time to next clock, this option will operate to 170 MHz using the typical AC parameters from the databook. As this is the limiting speed for the refresh counter, the external refresh connection is provided in the event that the remainder of the circuit should run faster.

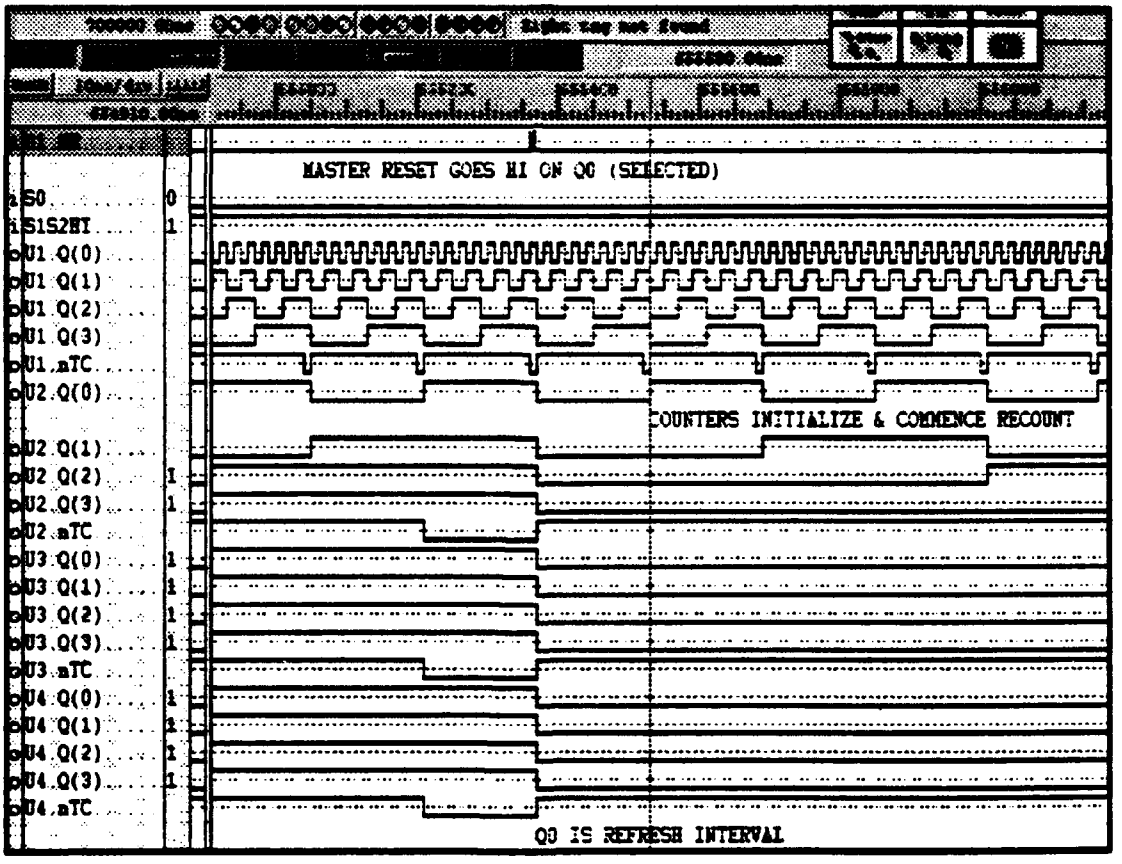


Figure 2-5 Refresh Counter Reset Sequence

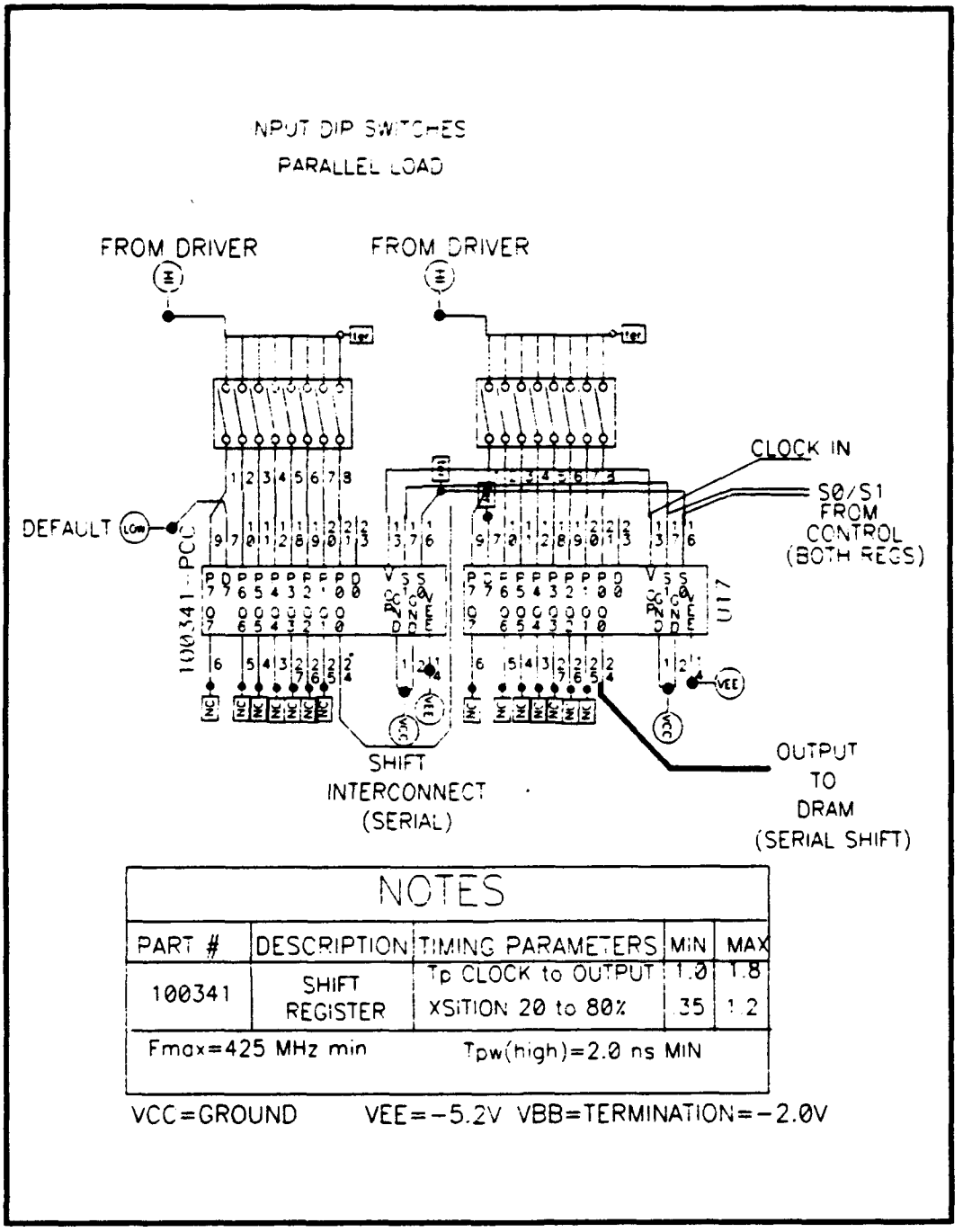
2. The Register Groups

There are four register blocks within the design consisting of the address registers, the READ/WRITE registers, the input registers, and the output registers. As stated, all parallel load from eight position DIP switches and then serially shift their data into or out of the DRAM. The four data input and four data output registers each hold eight bits (enough to fill the DRAM array). The remaining registers are staged to hold sixteen bits (to fill and then empty the array).

The READ and WRITE switches should be the complement of each other, other switches are set according to the data and addresses wanted. A functional schematic, Figure 2-6, is shown on the following page of a sixteen bit register group. DIP settings are presented to the preload inputs of the registers and the registers right-shift their data from Q0 into the DRAM based on control signals S0 and S1. A default bit is connected to the most significant bit position to force the final state of the machine to be a DRAM READ after all sixteen bits have been shifted out of the counters.

3. The Control Group

The control group includes both the manual/load switch unit and the register control logic. The hand switch consists of a DPDT switch that feeds a flip flop (to debounce the switch). The flip flop outputs to a counter/register that serially shifts the pulse out to the various registers. Using the counter/register synchronizes the manual switch with the system clock and should account for any metastability problems. The load switch prevents the system clock from entering the register groups, allows all load operations to be clocked from the manual switch, and provides the LOW signal to all register S1 control inputs for loading.



NOTES				
PART #	DESCRIPTION	TIMING PARAMETERS	MIN	MAX
100341	SHIFT REGISTER	Tp CLOCK to OUTPUT	1.0	1.8
		XSITION 20 to 80%	.35	1.2
Fmax=425 MHz min		Tpw(high)=2.0 ns MIN		

VCC=GROUND VEE=−5.2V VBB=TERMINATION=−2.0V

Figure 2-6 Schematic of Serially Connected Register Block

Register control consists of READ, WRITE, and DRDY. The truth table for the registers is shown below in Table 2-4 that shows the control states for the registers. The logic all triggers on a rising clock edge. Table 2-5 lists all the control logic states for the registers that are generated by a combination of READ, WRITE, and DRDY.

TABLE 2-4 TRUTH TABLE FOR REGISTER CONTROL

FUNCTION	S1	S2	CLOCK
LOAD REGISTER	LO	LO	⎍
SHIFT RIGHT	HI	LO	⎍
HOLD	HI	HI	XX
HOLD	XX	XX	HI
HOLD	XX	XX	LOW

TABLE 2-5 TRUTH TABLE FOR CONTROL LOGIC

READ (I)	WRITE (I)	DRDY (I)	INPUTSR (O)	OUTPUTSR (O)	DAS
LO	LO	LO	HI	LO	LO
LO	LO	HI	HI	LO	LO
LO	HI	LO	HI	LO	HI
LO	HI	HI	HI	LO	HI
HI	LO	LO	LO	LO	LO
HI	LO	HI	HI	HI	LO
HI	HI	LO	HI	LO	HI
HI	HI	HI	HI	LO	HI

The control logic works in the following manner. When a WRITE is presented, the data is strobed into the DRAM with the falling edge of data strobe (DAS) which is a delayed (WRITE)•(CLOCK). If a READ is presented and data is ready (DRDY) then the output registers shift right to accept the data, and the input registers shift right to present the next instruction. If data is not ready then all registers go into hold. The logic statements are INPUTSR=WRITE+nREAD+DRDY, OUTPUTSR= WRITE

+nREAD+nDRDY, and DAS=(WRITE)•(CLOCK). The schematic for the control is shown in Figure 2-7. For reference, the 100302 is an OR/NOR gate, the 100304 an AND/NAND gate.

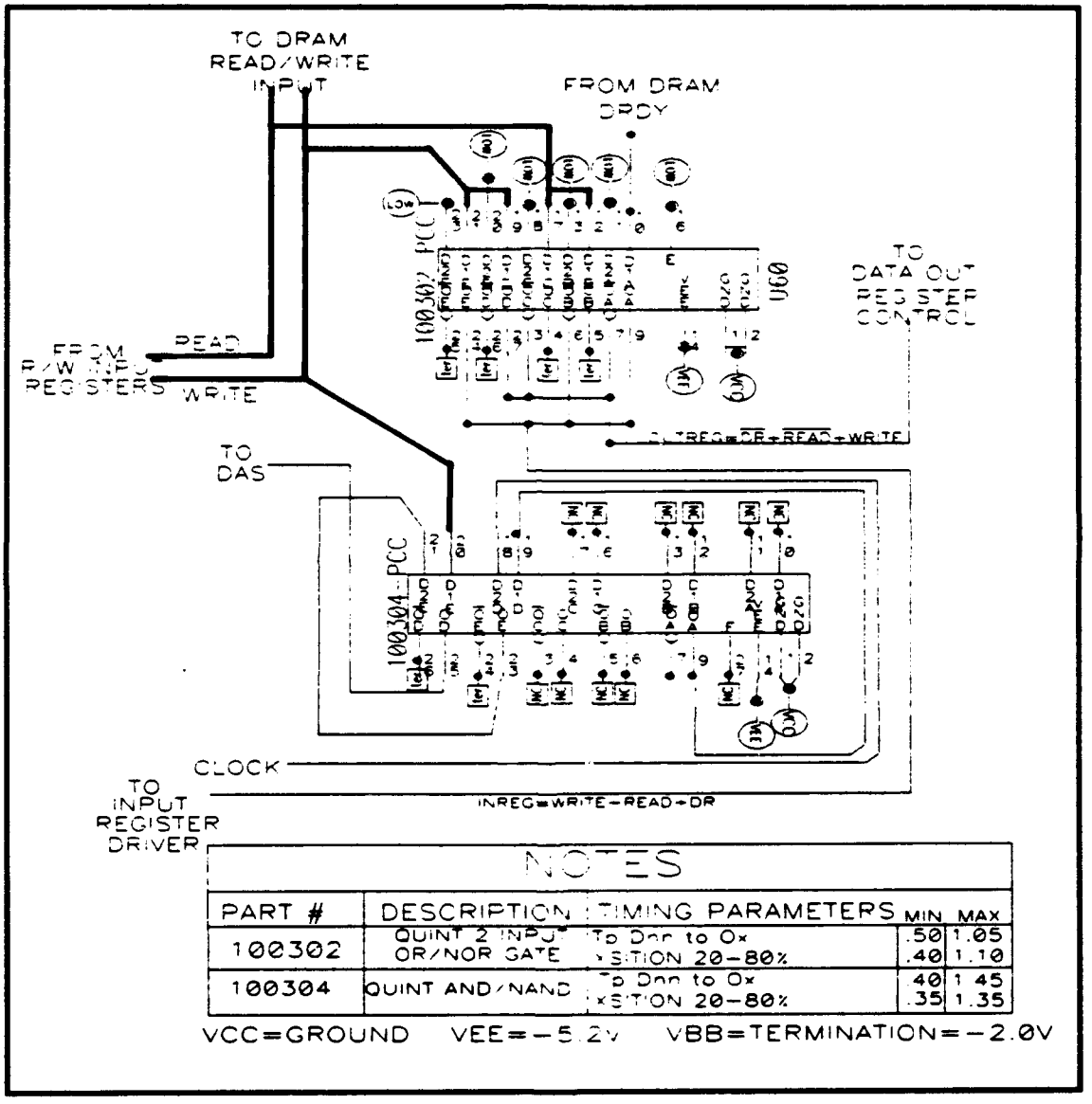
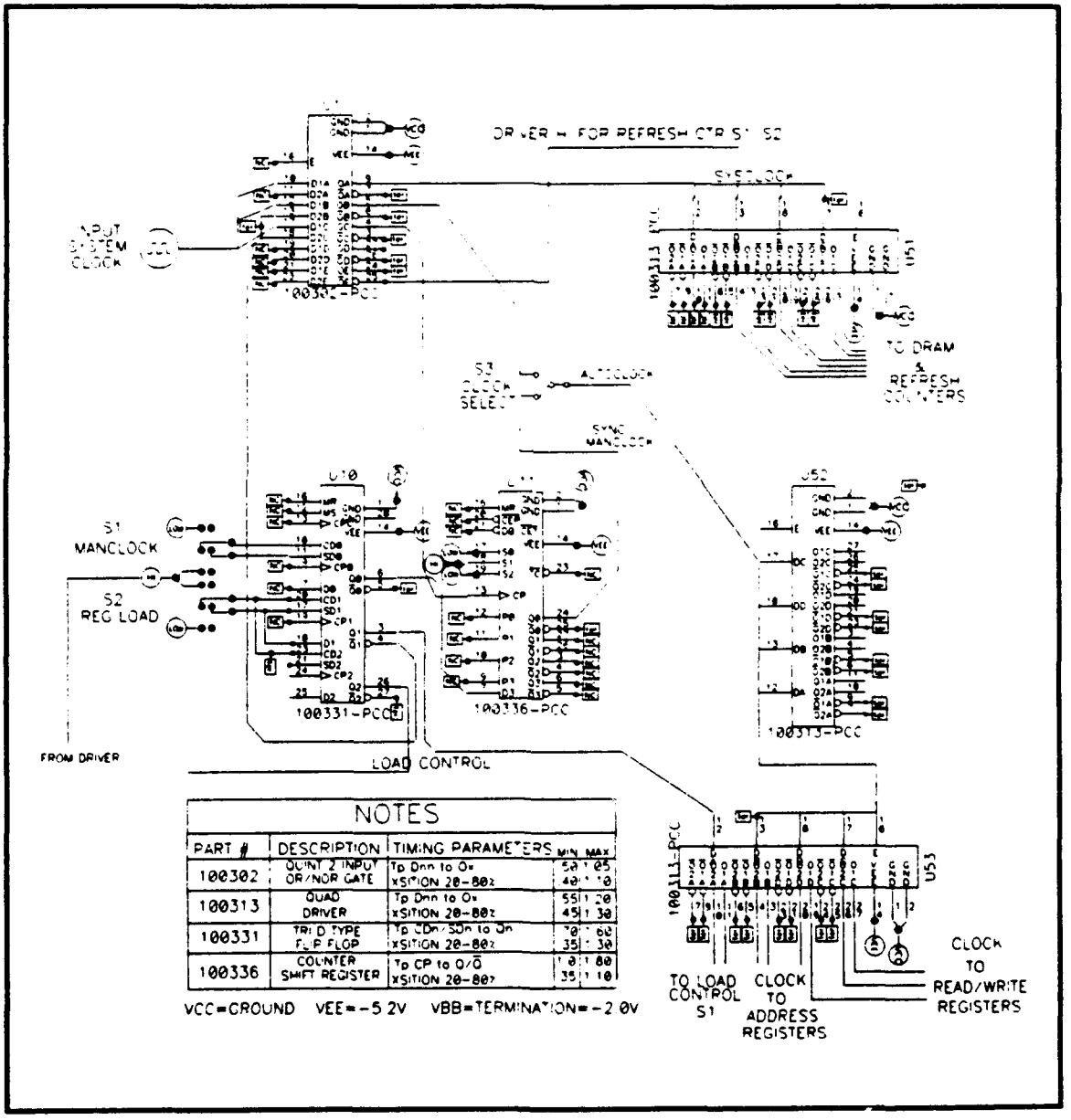


Figure 2-7 Register Control

Figure 2-8 is a diagram of the hand clock (MANCLOCK-S1), load control switch (LOAD-S2), and clock select (CLKSEL-S3). For reference the 100331 is a triple flip flop, the 100336 is a counter/shift register, and the remainder are OR/NOR driver circuits for the clocks.



PART #	DESCRIPTION	TIMING PARAMETERS	MIN	MAX
100302	QUINT 2 INPUT OR/NOR GATE	Tp Dnn to On xSITION 20-80z	5.0	10.5
			4.0	10.0
100313	QUAD DRIVER	Tp Dnn to On xSITION 20-80z	5.5	12.0
			4.5	13.0
100331	TRI D TYPE FLIP FLOP	Tp CDn/SDn to Qn xSITION 20-80z	7.0	16.0
			3.5	13.0
100336	COUNTER SHIFT REGISTER	Tp CP to Q/Q̄ xSITION 20-80z	10.0	18.0
			3.5	11.0

Figure 2-8 Manual Clock and Drivers

In addition to the circuits already discussed there are two additional OR/NOR logic drivers that provide only HI signals to the required control inputs. This is required because ECL cannot be connected directly to a voltage source due to the levels involved and must be fed from a logic gate. Also, any additional unused gates were utilized for the purpose of generating static logic to keep the fanout to a minimum throughout the design.

4. State Diagram and Operations Sequence

This section describes the sequence of circuit operation and references the state diagram, Figure 2-9, to show general operation. To set up a test, power is applied to the board and the onboard toggle switches are set as in the NOTES section (the fourth switch selects substrate voltage to the DRAM and is not shown). All registers are set with the desired data and then MANCLOCK is set high to load all registers. At this point the system clock (at working ECL frequency) is turned on at an external clock generator and the refresh counter will commence operation.

If manual switch option is needed, keep S3 in MANUAL, move LOAD to HIGH, then use the toggle to shift the registers. Shift operations will happen on the rising edge of each clock. High speed operation is accomplished by changing switch S3 to AUTO and the LOAD switch to HIGH. This allows AUTOCLOCK to drive all the registers and control system at ECL speed with operations completed (hopefully) in 60 nanoseconds.

The control system reacts according to the operations in the READ / WRITE registers. A WRITE (READ register=Ø, WRITE register=1) will set up the DRAM circuitry to accept data and produce a delayed pulse through the control logic for DAS. All input registers then shift right to the next operand. A READ (READ register=1, WRITE register=Ø) will check the DRDY signal. If data is not ready, then all registers

will go into a HOLD. Once the data is ready, the output registers shift right to accept data from the DRAM, and the input registers shift right to the next operand. A NO-OP (both READ and WRITE=Ø) causes a shift to the next operand.

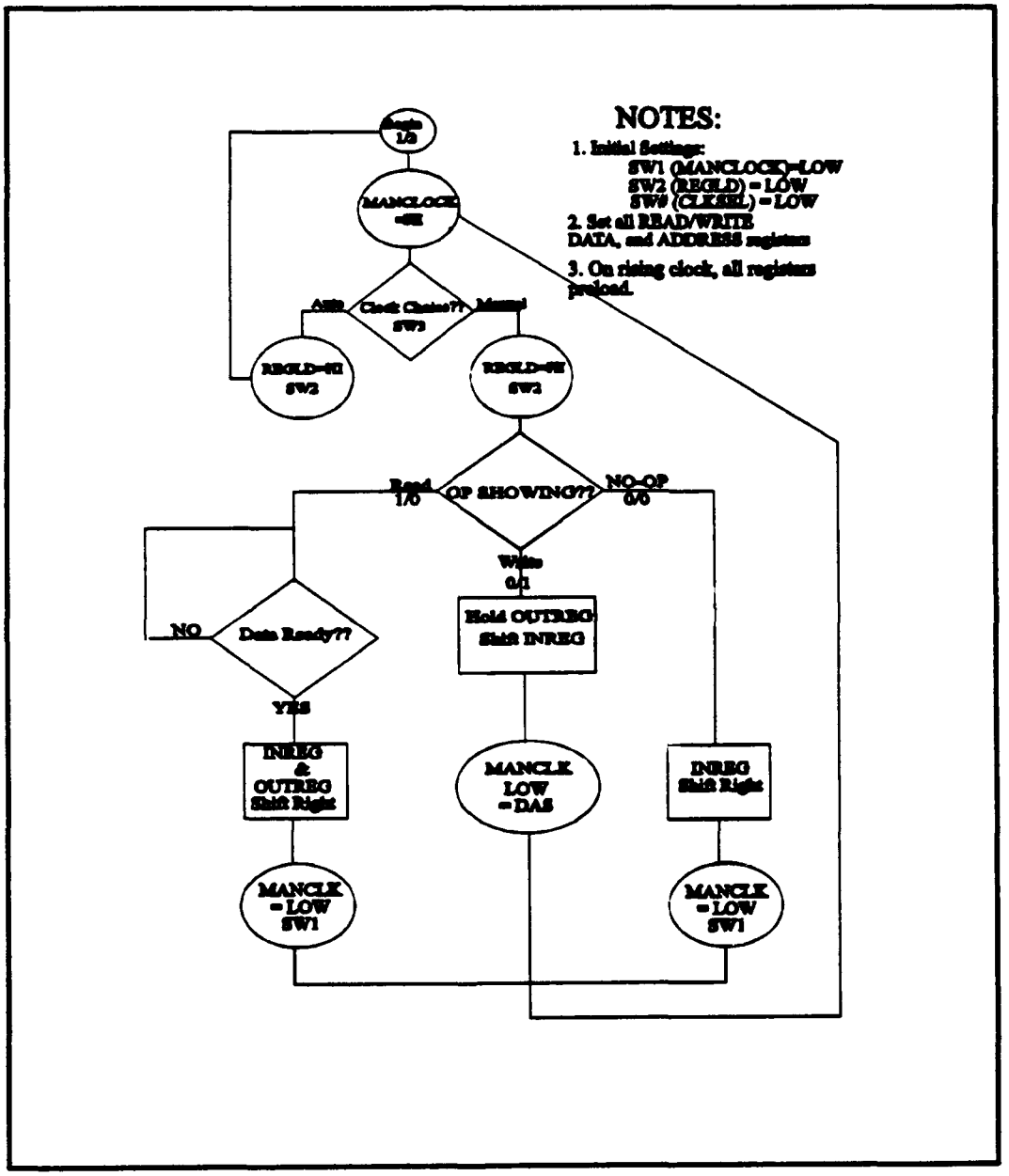


Figure 2-9 Logic State Diagram

III. EMITTER COUPLED LOGIC

The interface circuitry from the GaAs DRAM to the circuit board is composed of the chip input/output (I/O) pads that are ECL compatible. The pads convert the gallium arsenide voltage levels on chip to Emitter Coupled Logic levels at the package output pins. This chapter is devoted to characteristics of the ECL logic family and specific areas that relate to the PCB design.

A newcomer to circuit design with high speed logic families will not find many references in textbooks; locating some practical examples using ECL was a problem. The databooks and system design books [Ref. 5] initially available were helpful in gaining a basic understanding, but not of the broad range needed for a novice. As stated [Ref. 8] by Mr. Lee Ritchey, MAXTOR's chief of PCB/IC technology, "The Motorola handbook is still the only reasonable reference book for anyone wanting to do high speed design, and it is more than 20 years old." From the serious designer of high speed PCB's to someone wishing an introduction, the *MECL SYSTEM DESIGN HANDBOOK* [Ref. 9] has more information and answers more questions than any other source. The majority of this chapter uses that source as reference unless discussion of the specific IC's from National Semiconductor is presented.

A. ECL-HISTORY AND CHARACTERISTICS

ECL technology has been inclined toward serious systems designers and research applications due to the specialized need for logic operating in the 200-300 MHz range. However, with the introduction of faster systems and increased speed requirements ECL logic chips (albeit of the slower ECL families) are available at local electronics

suppliers. They include specialized transceivers that will convert ECL to any of the TTL logic families and even ECL logic with TTL compatable I/O pads.

ECL has been available as a logic family since the early 1960's. Typical gate propagation delays were 8 nsec with toggle rates approaching 30MHz. [Ref. 9]. Considering historical speed requirements, the technology was very capable and used extensively in specialized applications well into the 1970's. Further developments in the late 1960's refined ECL technology to gate delays of 1 ns and clock rates of greater than 500MHz . Today, commercial ECL semiconductors are available that offer .33 ns propagation delays and operating frequencies over 1.1 GHz. that are competitively priced with more advanced TTL families.

Access to a logic family with operating frequencies that provide the fastest speed IC logic available seems irresistible to system designers. However, there are many factors that have discouraged widespread use of ECL. Foremost is ECL uses negative voltages for logic level and exhibits a typical voltage swing of 800 mV (-.89 V = LOGIC '1' and -1.7 V = LOGIC 'Ø'). Power supply requirements consist of 0 V as the high and -4.5 to -5.2 V as the low voltage references. Additionally, a return supply of approximately -2.0 V is required to provided proper output level shifting for the ECL circuit as the termination voltage for impedance matching. A major disadvantage is high power consumption and thermal characteristics. The incompatibilities and the extra power supplies have tended to discourage use of this technology in commercial applications and current architecture's. However, new IC's are available that combine TTL/ECL technology and translation on the same integrated circuit and newer IC versions are being introduced with reduced power requirements. Table 3-1 is presented to compare ECL products with the other logic families with a statement of the current state of ECL

in the introduction to National Semiconductor's new F100K 300 Series databook [Ref. 7] as follows:

> Precious few alternatives offer the performance of ECL. Most designers recognize the advantages offered by ECL in high speed systems extend beyond just quick switching times. However, the use of ECL has been somewhat limited to those applications concerned with high speed and often little more. These applications usually had extravagant cooling systems and massive power sources to keep the signal moving. Rapid advancements in microprocessors and high resolution video equipment are now beginning to push the preferred TTL and CMOS technologies to their limits. The need for functions with ECL-like speeds without ECL-like power for use in smaller but increasing powerful systems is growing rapidly". "However, the majority of designers never had to consider ECL until now. The increasing availability of high speed microprocessors is driving the need for faster busses and more accurate clocking.

TABLE 3-1 COMPARISON OF LOGIC FAMILY CHARACTERISTICS

DESIGN FAMILY	CIRCA	CLOCK FREQUENCY	PROPAGATION DELAY	STATIC POWER DISSIPATION	*NOTES*
TTL 74	1963	35 MHz	10 ns	10 mw	
TTL 74LS		40 MHz	10 ns	2 mw	
TTL 74AS		180 MHz	3 ns	8.5 mw	
TTL 74ALS		70 MHz	6 ns	1 mw	
CMOS 74HC		40 MHz	7 ns	25 nw	
MECL III	1968	min 500 MHz	1.0 ns	60 mw	Motorola
MECL 10,100	1971	min 125 MHz	3.5 ns	25 mw	Motorola
MECL 10,200	1973	min 200 MHz	2.5 ns	25 mw	Motorola
MECL 10KH	1981	min 250 MHz	1.8 ns	25 mw	Motorola
F100K ECL	1974	400-500 MHz	.75 ns	35 mw	Fairchild
F100K ECL 300	1991	400-500 MHz	.75 ns	19 mw	National
MECLinPS	1987	1100 MHz	.33 ns	26 mw	Motorola

The F100K family from Fairchild seems the most referenced high speed ECL product. National continued to make the F100K series after Fairchild ceased operations and has now introduced an update to the original F100K that is identical in package layout but with better power characteristics (F100K 300 Series). These are the IC's chosen for our project as they were readily available in a surface mount package.

B. WHAT IS HIGH SPEED?

Current popular literature [Ref. 8, 10] describe a "high-speed circuit" as one with clock rates of over 50 MHz. Many who are operating 33/66 MHz personal computers in their homes may consider that figure somewhat conservative. For those new to design, seeing ECL IC's capable of 400 MHz gives rise to the question **"what really is fast?"**. A quote from the MECL System Design Handbook [Ref. 9] puts it in perspective:

> Any signal path on a circuit board may be considered a form of transmission line. If the line propagation delay is short with respect to the rise time of the signal, any reflections are masked during the rise time and are not seen as overshoot or ringing. As a result, because of the high ratio of rise time to propagation delay time, signal lines for most MOS circuits may be several feet long without signal distortion. However, as edge speeds increase with faster forms of logic, the line lengths must be shorter in order to retain signal integrity.

The bottom line is that edge speed vs. interconnect length determines if a circuit should be considered high speed. It is of enough consequence that the MOTOROLA 10K ECL SERIES was modified to lengthen edge rates to over 3 nsec [Ref. 9]. Once the logic transition time is less than the propagation of the signal from source to load you have reached a transmission line environment. The step function harmonics of the logic pulse also contribute to the noise environment within the transmission line and are generated at such high frequencies that crosstalk between lines can contribute to the design problem.

Solutions to the problem are all related to maintaining a characteristic impedance throughout the environment with the termination resistors and matching the transmission line itself to the board environment. The use of ground planes and power planes to sink stray emissions from the line has a major influence on signal integrity.

Transmission line effects increase design and manufacturing costs. Speed predicates the use of impedance matched coaxial cable or multilayered circuit boards with multiple ground plane for a complex circuit. From comparison of the board cost for this project, a multilayer PCB may be as many as four to five times more expensive than an equivalent size double-sided circuit board.

C. TRANSMISSION LINE INTERCONNECTIONS

Once it is determined that a transmission line effect may be present, the designer has options in how to implement the requirements. Additionally, other than the geometry of implementation there are other factors that will impact how a printed circuit or breadboard design will progress. All of these factors will be based on maintaining a constant characteristic impedance (Z_o) over the length of the circuit. For the purposes of this project and standard with most ECL applications, a Z_o of 50Ω was chosen.

To recap the requirements for ECL components the following rules for a standard logic interconnection are listed with an example circuit shown in Figure 3-1. Only parallel line termination will be discussed as it was exclusively used in the design and stripline architecture (to be discussed later) will be used as an example.

- Power requirements (labeling scheme depends on manufacturer):
  - most positive voltage = ground (labeled VCC or GND).
  - most negative voltage = -4.5 to -5.2 V (labeled as VEE).
  - voltage for termination resistor = -2.0V (labeled as VBB/VTT)
- The signal lines are terminated at the end with a resistor of 50Ω. The signal line itself will have a geometry that supports 50Ω impedance. The terminating resistor will be connected as close as possible to the load input with the other end connected to -2.0V. If the line is short (as feedback into the same package), the line may remain unterminated. This

is discussed in the data book and would be limited to a length of less than one inch for a single load to less than 0.4 inches with a fanout of four.

- Unused inputs/outputs are left unconnected. If an output is used, the associated complement terminal should be terminated.
- The package is connected to VEE and VCC (GND). The end of the resistor (labeled TER) would be connected to the -2.0 V supply.

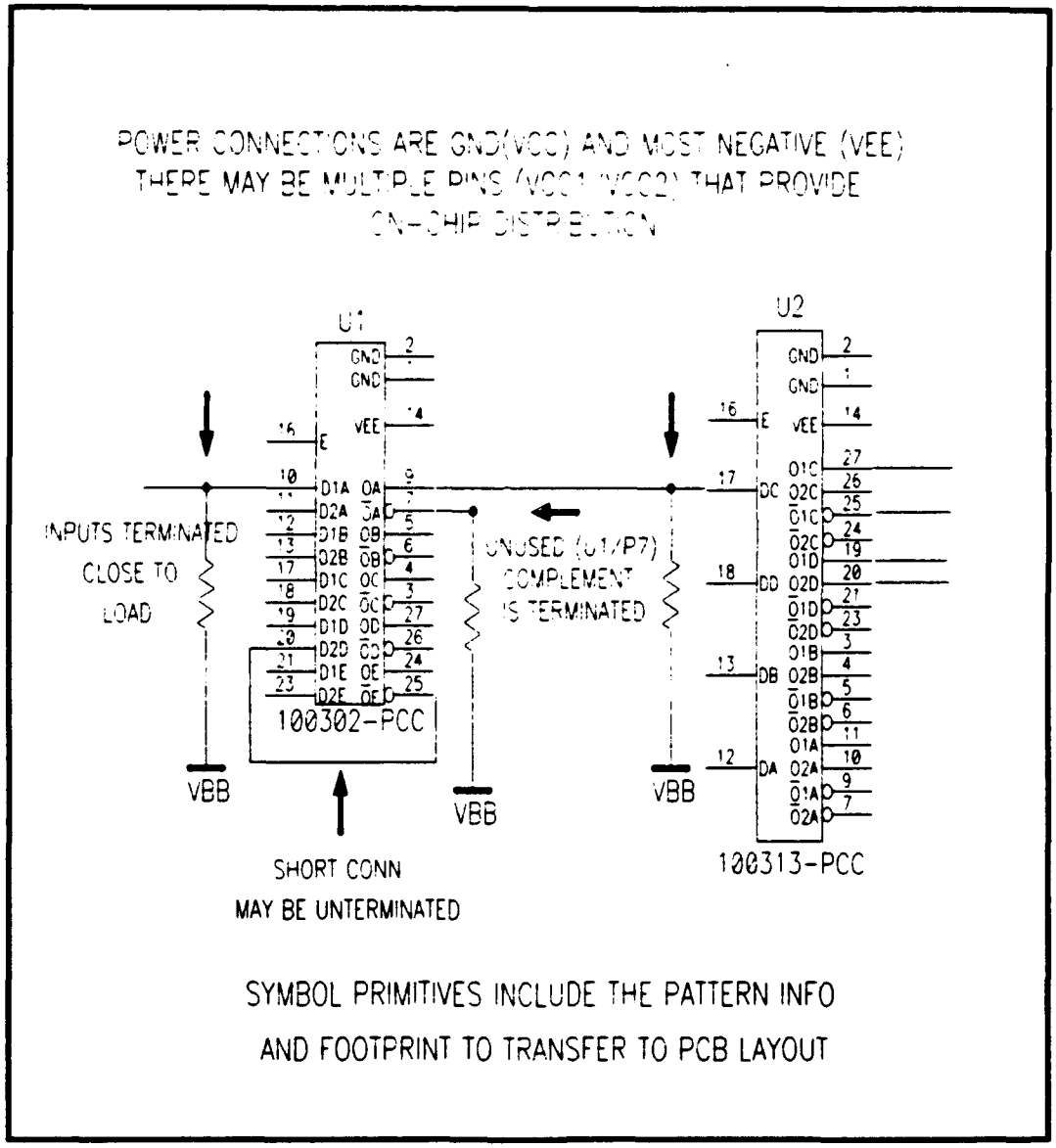


Figure 3-1 Examples of ECL Connection Rules

D. ECL DESIGN CALCULATIONS

To show the above design rules in practice, the calculations that would be required by the designer and the printed circuit manufacturing house are presented in this section. These will be specific to the project board but many configurations are availiable depending on the application. For example, if the board were required to fit in a computer slot, it's total thickness would be 625 mils which would impact all other aspects of the design. If it were required to be 1000 mils due to vibration, then another set of configurations would be considered. As the project board has only to maintain the 50Ω matched impedance, it will have easier defining calculations.

First, we have to show the geometry that is used. In this case it is known as the stripline architecture, and is the most expensive of the common applications (others are microstrip, wire over ground, twisted pair, coax, etc). Figure 3-2 below shows an example of the high-speed signal layer between a ground and power plane (as layer MID2 shown in Appendix A):

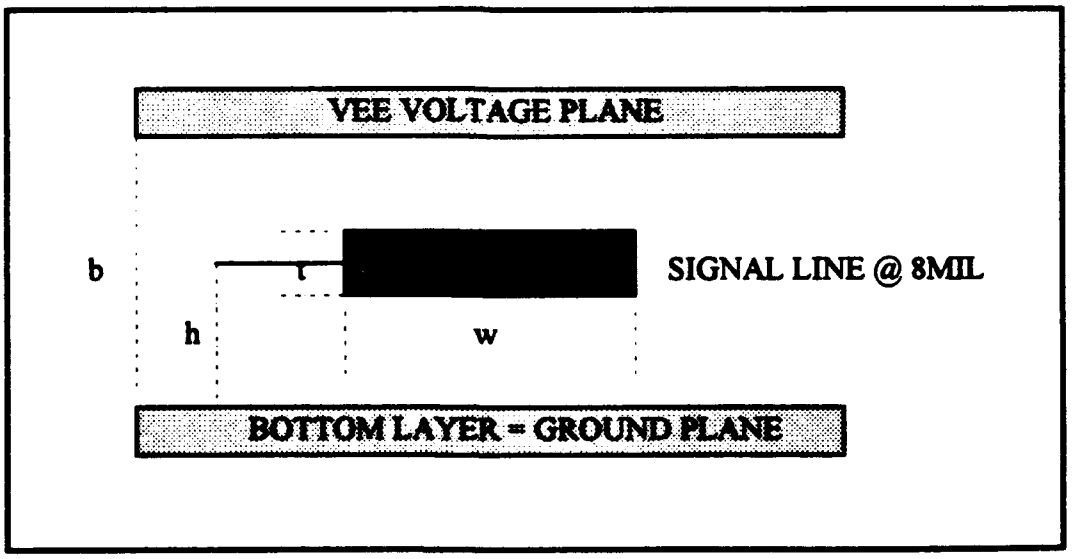


Figure 3-2 Stripline Architecture and Dimensions

Using the dimensions shown in Figure 3-2, the overall remaining dimension of the circuit board may be calculated. We enter the calculations with the 8 mil signal lines on ½ oz copper (6 mil), a 50Ω impedance requirement, and use of G-10 epoxy glass (a standard and inexpensive board material) as the board laminate. The relative dielectric constant (E_r) of G-10 is 5.0. However, 4.0 will be used to correct for operating frequency of 200MHz. This figure must also be combined with the E_r of the material between the laminates. That factor will have to be determined by the board fabricator to yield the best match of the 50Ω impedance. The equations [Ref. 9] are:

From Figure 5.2 and the values given, the following formulas are used to find the distance between the layers:

$Z_o = 50 \qquad E_r = 4.0 \qquad w = .008\ inches \qquad t = .0006\ inches$

$$b = \frac{e^{\left(\frac{Z_0 \times \sqrt{E_R}}{60}\right)}}{4} \times \left(.67 \times \pi \times \left((.8 \times w) + t\right)\right)$$

$b = 0.0195\ inches$ This is the distance between the planes.

$$h = \frac{b}{2}$$

$h = 0.00975\ inches$ This is the distance between stripline center and adjoining planes.

$h1 = h - .0006$

$h1 = 0.00915$ This is the dielectric thickness between layers with stripline height accounted for.

The board is six layers:

LAYER 1 = TOP SIGNAL = 1oz COPPER = 1.2mil
LAYER 2 = POWER (VBB) = 1oz COPPER = 1.2mil
LAYER 3 = MID1 (HIGH SPEED) = .5oz COPPER = 0.6mil
LAYER 4 = POWER (VEE) = 1oz COPPER = 1.2mil
LAYER 5 = MID2 (HIGH SPEED) = .5oz COPPER = 0.6mil
LAYER 6 = GROUND = 1oz COPPER = 1.2mil

$$\text{Total Thickness} = (.0012 \times 4) + (.0006 \times 2) + (h1 \times 4) + (.003) + (.0055)$$

Thickness = 0.0511 *inches*

Total board thickness is approximatly 50mils by addition of the 6 layers, the 4 layers of dielectric for high speed, 1 5.5mil layer between TOP / VBB layer, and a standard 3mil allowance for hole plating thickness (1.5 mil per side).

Base Equation for the above [Ref. 9]:

$$Z_0 = \frac{60}{\sqrt{E_r}} \times \ln\left[\frac{4 \cdot b}{.67 \times \pi \times w\left(.8 + \frac{t}{w}\right)}\right]$$

The information provided by the "board house" that was contacted for allowable tolerances gave a total thickness of 50.0 mils for the total project. Note that the 5.5 mil dielectric between TOP and VBB was chosen by the board house to reach a standard 50 mil thickness overall. There were a number of iterations of this calculation due to the fact that they do not normally run the signals between power and ground planes. The usual practice would be to put the VBB and VEE planes together and then mate MID1 and MID2 to give a standard thickness of 62 mils. However, that would be better suited to the microstrip architecture used in slower circuits.

Figure 3-3 on the following page shows the final layout along with an example of a via that is attached to the VEE power plane. The software only allows this type of via that transverses all board layers. A more expensive technique uses "buried vias" which only connect between layers where necessary and can save on the total area on the top and bottom of the board to mount components (as each via in the project setup requires 30 mil of clearance to any other structure). Note that the software tracks the size of the via, the required clearance around the via, the distance to adjacent lines of the same layer, clearance between surface pads (that are common to top or bottom only), and the clearance around thru-hole pads (that extend through all layers as a via).

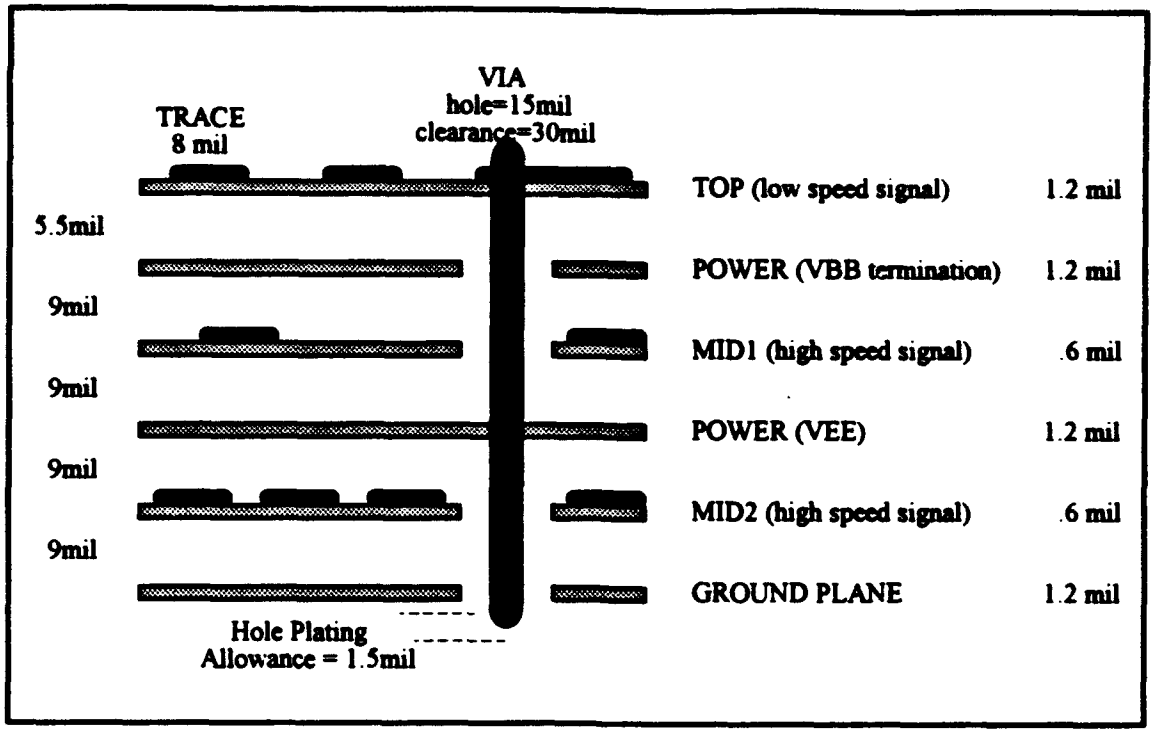


Figure 3-3 Board Layers and Tolerances

The next set of calculations give the base propagation delay of a signal moving along a trace on a strip line and the maximum length of line allowed from termination before reflection will take place back down the line. [Ref. 9]

$$t_{propagation} = 1.017\sqrt{e_r}\ n\text{sec per foot} \qquad l_{max} = \frac{t_{rise}}{2 \times t_{propagation}}$$

The values provided by the previous equations provide a propagation delay of 2.23 nsec/ft and a maximum unterminated line length of 2.01 inches based upon a rise time of .75 nsec for the National Semiconductor 300 Series.

The maximum unterminated line length is then adjusted by the amount of loading on the line. All databooks present various levels of the equations involved and then provide the final values for loading. The equations lump capacitance for each load and

relate it to the capacitance of the trace to provide a final l_{max}. The final values for the project components used are provided in Table 3-2.

TABLE 3-2 UNTERMINATED LINE LENGTH ALLOWANCES-NATIONAL 300 SERIES

Z0	1 LOAD	2 LOADS	3 LOADS	4 LOADS
50Ω	.94"	.68"	.52"	.41"
62Ω	.87"	.59"	.44"	.34"
75Ω	.79"	.52"	.37"	.29"
90Ω	.72"	.45"	.32"	.25"
100Ω	.68"	.41"	.29"	.22"

What table 3-2 shows is that with the increased number of loads the final termination has strict requirements as to the distance from the terminating resistor to the final load on the line. When the size of the circuit board and the SMT component size is considered these distances are not difficult to maintain in a custom design.

This concludes the discussion on ECL and some of the general design rules. There are many more complications and areas that need to be studied prior to commencing ECL design, however the basics have been presented to give a general overview of the project. The databooks all have the same basic information in them but the *MECL System Design Handbook* has a full discussion of each topic from the nomograms to the differential equations.

IV. TEST CIRCUIT IMPLEMENTATION

All the prior documentation is centered on reaching this point in the presentation. The combination of the logic design and the circuit theory must all come together to produce a product. It was suprising how little information is available in reference material and also interesting to see how recent publications were already out dated by current technology in regard to PCB manufacture.

This chapter will discuss the software utilized and process of getting to final proofs for fabrication. For reference, a copy of the photoplotted layers of the circuit board are included in Appendix A. A selection of the more relevant report outputs of the PCB program are included in Appendix B. If ever there were "lessons learned", they were encountered throughout the PCB layout process. This chapter is also designed to be documentation for the PCB design for reference and manufacture. As the entire process is intricately interwoven with the software products used, the discussion will begin there.

A. SOFTWARE FOR PCB AND LOGIC DESIGN

There were four Computer Aided Design (CAD) / Computer Aided Manufacturing (CAM) products used during this phase of the project. The schematic capture, PCB layout, and PCB autorouter were all TANGO products [Ref. 11, 12, 13] and are very popular on the commercial market. The SUSIE-CAD simulator has already been introduced in Chapter II.

The schematic capture program (which produced the circuit diagrams for this report) can only be rated as outstanding. It kept track of all design errors and insured that the actual design was properly fed to the PCB layout program. The libraries did contain the older NATIONAL ECL parts, and all had to be modified (several times) to

fit the packages that were ultimately used. With the design drawn, a netlist was post-processed by the program along with design errors to enable error correction.

Once the schematic was complete, a netlist was produced and sent to the PCB layout program. This product was also outstanding. There is not a great deal of automation as far as placing components but it does keep track of all the connections and performs a superior design check of critical clearances at all board layers. The final product produced twelve layers of output that cover everything from documentation and silkscreen masks, to signal lines and solid copper planes. It is capable of tracking a total of two planes, ten signal layers, and eleven layers of board for documentation and CAM (total 23). This project had different requirements as far as solid planes, but the software was capable of being modified to handle the differences. Essentially the VBB termination voltage plane and VCC power plane were assigned to the two automatically produced planes. The bottom ground plane had to be hand drawn. That does not sound difficult but every part of the ground plane had to maintain 10 mil tolerance from any part, via, or thru-pad. There are 800 holes of this type on the board so the ground plane took days to draw and then get a final design check.

There were great hopes for the autorouter, but this project was far beyond it's capability. There is no doubt that it could do a satisfactory job on a more conventional design, but it never produced anything of merit with the close package density required for minimum line delay. Additionally, the required third solid plane was not something the autorouter was designed to handle. Workarounds were used, but all autorouted output was ultimately discarded.

The software used is a major portion of success in accomplishing this type of design as it can only be accomplished by computer. The line widths and tolerances are beyond

human capacity to produce by hand. Table 4-1 shows that there are too many variables to be tracked on an area of 56 square inches.

TABLE 4-1 PRINTED CIRCUIT BOARD STATISTICS

ATTRIBUTE	DESCRIPTION	VALUE	NOTES
Technology	SURFACE MOUNT		
Dimensions	Width	8.5 in.	
	Depth	7 in.	
	Thickness	52.8 mils	*3 mil for hole plating
Layers	1. Low Speed Signal/Surface	1.2 mil thick	1 oz copper
	2. Voltage Plane VBB termination	1.2 mil thick	1 oz copper
	3. High Speed Signal (MID1)	.6 mil thick	.5 oz copper
	4. Voltage Plane VEE	1.2 mil thick	1 oz copper
	5. High Speed Signal(Mid2)	.6 mil thick	.5 oz copper
	6. Bottom Voltage Plane (GND)	1.2 mil thick	1 oz copper
	7. Dielectric Thickness	9 mil	5 layers
Components	34 28-pin PLCC IC's	300 Series ECL	National Semiconductor
	Resistors (termination)	150	surface mount 1206
	Capacitors(bypass)	69	surface mount 1206
	1 132-pin PLCC		GaAs DRAM
	4 switches		
Line Width	All signals	8 mil	
Total Lines	Signal + Bottom Plane Fill	8-10-12-20-100	>5000 line segments
Total Vias	Includes Vias+GND Plane Conn	464	vias 30 mil x 15 mil hole
Total Holes	Vias+ThruPads to Planes	780	hole clearance @30 mils
VBB Connect	Connections to VBB Plane	186	resistors + bypass caps
VEE Connect	Connection to VEE Plane	100	bypass caps+chip power
Design Rules	Clearance Pad to Pad	10 mil	
	Clearance Pad to Line	10 mil	
	Clearance Line to Line	10 mil	
	Clearance Hole to Hole	30 mil	

B. SURFACE MOUNT TECHNOLOGY

Surface Mount Technology (SMT) is the state of the art in PCB design. The growth in SMT use was a consideration in the components, manufacturer, and package type used in the design. Contacts with semiconductor companies indicated that the parts necessary (in such a small lot) may not be available for months.

The *TANGO* software fully supports SMT technology, and each component is coded with a pattern in the schematic capture program. However, even the simplest design will probably encounter a lack of necessary library patterns. The manufacturer must be contacted or the dimensions can be taken from databooks. The more difficult pattern is the one for SMT switches and auxiliary components that are purchased from a distributor, however the manufacturer will provide a "footprint" on request. The best alternative is to have an example of the package that can be tested to "homemade" surface mount patterns.

The advantages of SMT are numerous [Ref. 14]. By having the component mounted on either the top or bottom of the board opens significantly more area. The lack of thru-hole connections allows signals to be routed under components without the via interference that would be present in a normal design. Package geometry can be better designed for performance of integrated circuits by moving away from the rectangular DIP packages to square flat-paks and Plastic Leaded Chip Carriers (PLCC). Additionally, a 132-pin DIP package would be extremely large in relation to the surface mount version. Table 4-2 [Ref. 14] lists some of the advantages and disadvantages that may be offered by SMT. Figure 4-1 shows the patterns that were used in the design of the project board to show the sizes involved in the design. A 24-pin DIP socket is included as a size reference for those unfamiliar with SMT.

TABLE 4-2 SELECTED ADVANTAGES AND DISADVANTAGES OF SMT

Advantages	Disadvantages
Size-a SMT board is 30-50% smaller	Integration yield higher thermal problems
Via area reduced by average factor of 3	Cost of market entry
Smaller components enables thinner board	Standards lacking for packages and design
Less parasitic capacitance due to leads	Size increases testing difficulty
High interconnectivity due to lead density	Density yields higher power dissipation/area

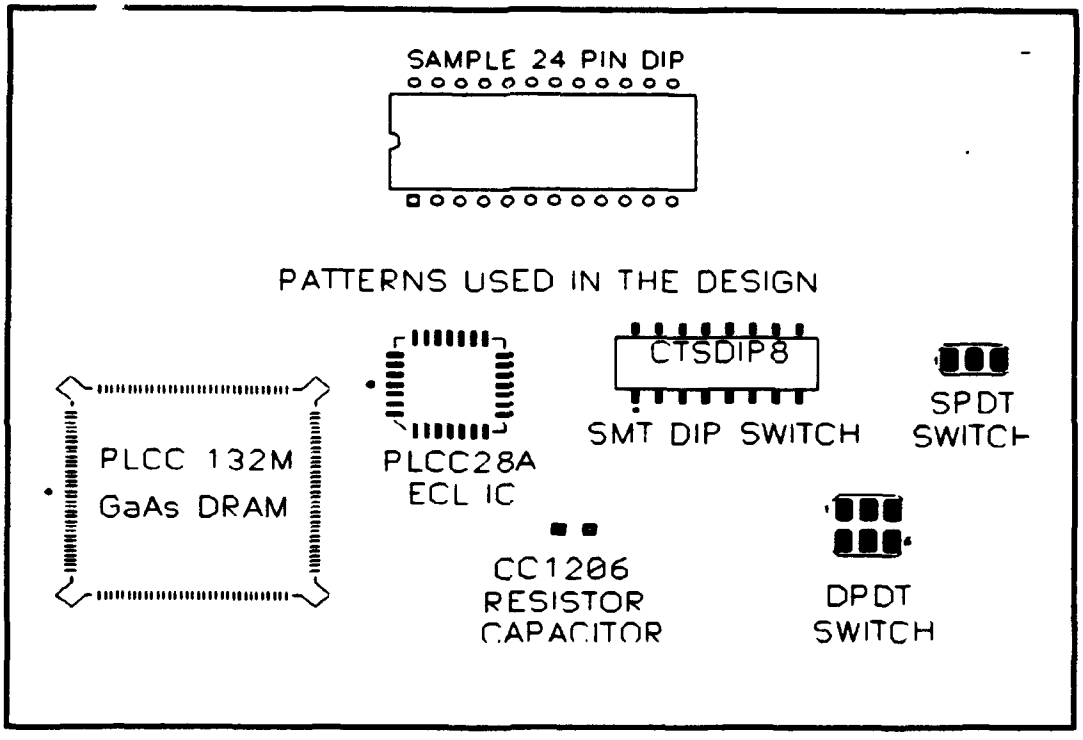


Figure 4-1 Sample SMT Patterns Used in PCB Design

C. THE PROCESS

In accomplishing initial research, there were few current books on this topic. The periodicals indicated that discussion of high-speed PCB design can be a heated topic. The best reference found was the *PRINTED CIRCUITS WORKBOOK SERIES*

[Ref. 14]. However, once a relationship had been established with a PCB manufacturer the five book series was already proved outdated. The dimensions that would be considered "daring" in 1990 were the first choice offered by the board house.

The designer of a high speed or multilayer product with high integration and tolerances should be working hand-in-hand with a PCB fabricator. The manufacturer's representatives will ask the questions that can improve a design and allow a feel for what can be accomplished. This board was planned to be routed with 12 mil signal lines until discussions were made with the manufacturer. The reduction to 8 mils made a major difference in the plan for overall dimensions. The figures shown in Table 4-1 were recommended by the manufacturer and were illustrated by calculation in Chapter III. With this information in hand the process of placing components and routing signals and interconnects commenced.

D. LAYOUT

When the layout phase of the board commenced, the pin-outs, and size of the GaAs DRAM were not known. A decision was made to allow 1.5 inches for that package to include enough room around it for soldering and any repair work or modifications. The method used to try to match the signal line length was to draw circles around the DRAM center and to try to place all input and output packages on the circular arc. That seemed to work well even after the DRAM pin description arrived, but it would have been advantageous to have placed the right signals on the correct side of the package.

The next step was to place the remainder of the packages on the board and commence routing. If there is a major problem in the design, it will be at this point. Numerous driver and clock packages in the logic design were optimized to use all the gates. However, once placed on the PCB they had long lines across the board which will have some skew impact. Despite the fact that 50% of the routing was complete, some of

the packages were moved and attempts were made to even out the clock signals to a uniform length.

Once all the integrated circuits were placed, the process of placing the terminating resistors and bypass capacitors began. It was a mistake to wait so long in the process to start this part because space was at a premium. It was only the SMT allowance of placing components on the underside of the board that allowed getting all components placed. As it is, the task of assembling and soldering will not be easy.

There was an attempt to stagger the IC packages on the top and bottom of the board. That would have allowed an even smaller design. However, there did not seem to be any organized way to make that happen and the hand drawn ground plane would have been ten times more difficult. Perhaps a more experienced artist could have found a way to accomplish that.

Once all parts were placed, the ground plane was drawn. A day was allowed for this but it took a week. By this time all the parts were placed and ground plane roughed in it took almost two hours for a complete design rule check on a 80386 computer. Each change required another run until all errors were corrected. Earlier in the design, the design rule check (DRC) option was producing over 70 pages of errors. The final run was less than a page of status items only. Appendix B shows some of the output produced at the end.

E. PREPARING FOR FABRICATION

The final step is the CAM output. The PCB program makes this very easy and is even a major improvement from it's prior release. The program produces photoplot files with the etch patterns, all hole sizes and locations, and tool assignments for the drill machine. The final step is to send these files to a board fabricator and wait for the result.

The board house that was used to help in design does accept one-of-a-kind projects like this but they prefer runs in the hundreds. Generally, the sales representatives feel that this is an opening for further business in the future. The cost of the circuit board will be in the area of nine-hundred dollars after tooling and design work is considered. That is with the caveat that the board will not be a priority and can be a filler in the schedule. Other fabricators need to be contacted to compare pricing.

V. CONCLUSIONS

A. THE SCOPE OF THE PROJECT

This task commenced with a plan to design the test fixture, manufacture it, and then operationally test the DRAM. The late delivery of the chip and it's pin information reduced the scope to just design of the logic and printed circuit board. That did not seem like much of a project, but in reality it became a "full plate".

Initial research included some wire-wrap ECL projects and etching two-sided PCB's using the educational versions of the software. Although they added to the experience, they had nothing to compare to the thirty component, six layer design that was the result of this project. If anything, they gave a false impression of the amount of work involved in a high-speed, multilayer circuit card design. Appreciation of the effort involved in this type of work is a major lesson.

The schematic and PCB software tools referenced are all outstanding products. All were stable and fast on an 80386 personal computer and the design rule checking was perfect as far as can be determined. Any discontent would be unfair because they were asked to go beyond what they were designed to do. Despite many hours with each product there are still secrets to be learned. One recommendation is to use another PCB program if more than two solid planes are required. Drawing the bottom ground plane by hand (to 10 mil tolerance) seemed the only option and was measured in days, not hours.

Library assets were one reason the simulator software was purchased. The schematic and PCB software also have extensive libraries. However, in the areas of ECL and surface mount technology, the vendor should be asked what models are offered and

in what package types. SMT footprints should also be requested early if a physical example or good engineering drawing is not available.

B. ENGINEERING CHANGES

As with all engineers, with experience, many things could be altered. The logic would not have many revisions but the interconnections between components would see major changes. Actually seeing the pieces on the circuit board caused alot of worry with respect to line delay. Redesign was done if it was considered a major problem. However, there are many smaller areas that could use improvement.

In a high speed application the length of interconnect lines has to be a priority. Actually, there needs to be some iteration between the logic design and placement on the PCB, but that knowledge has to come from experience. Alternatively, the plan for placing the components should have been more organized. There is enough room between the PCC's to solder and do any repairs, but stuffing the two-hundred terminating resistors and sixty capacitors on there too will make the soldering job a difficult project. It could be done much better.

C. THE KNOWLEDGE BASE

A surprising aspect of this project is that it is very specialized. The lack of references and current handbooks make this a difficult area to research. The *MECL SYSTEM DESIGN HANDBOOK* was the tool and is highly recommended for every engineer's library.

A trip to a board manufacturer was something that should have been done at the 50 percent point in the project. It would have solved many problems and opened many avenues of information to someone undertaking a project of this type. As stated in the

text, sources less than two years old will lead the inexperienced designer down the wrong path.

Understanding ECL was initially very hard. The technology has minimal exposure in the classroom or textbooks. Some basic experimentation and guidance made the mystery of ECL disappear. Additionally the difficult subjects of transmission lines, impedance matching, and high frequencies all seem to come together in a real world application of high speed printed circuits.

APPENDIX A

This section contains the photoplot proofs for the printed circuit board. Note that both the POWER (VBB termination voltage) and GROUND (VEE reference voltage) planes are plotted in the negative due to the software constraints. The BOTTOM layer, which is the true GROUND plane, is plotted in positive. The layers are labeled in order of their position as follows (actual size):

- Figure A-1 TOP ASSEMBLY LAYER
- Figure A-2 TOP SOLDER MASK
- Figure A-3 HOLES AND VIAS PLOT
- Figure A-4 TOP SILK SCREEN
- Figure A-5 TOP LAYER PADS AND SLOW SPEED SIGNAL
- Figure A-6 POWER=VBB TERMINATION (INNEGATIVE)
- Figure A-7 LAYER MID1=FIRST FAST SIGNAL LAYER
- Figure A-8 GROUND=VEE LAYER (PLANE IN NEGATIVE)
- Figure A-9 LAYER MID2=SECOND FAST SIGNAL LAYER
- Figure A-10 BOTTOM LAYER=TRUE GROUND PLANE
- Figure A-11 BOTTOM ASSEMBLY LAYER
- Figure A-12 BOTTOM SILK SCREEN

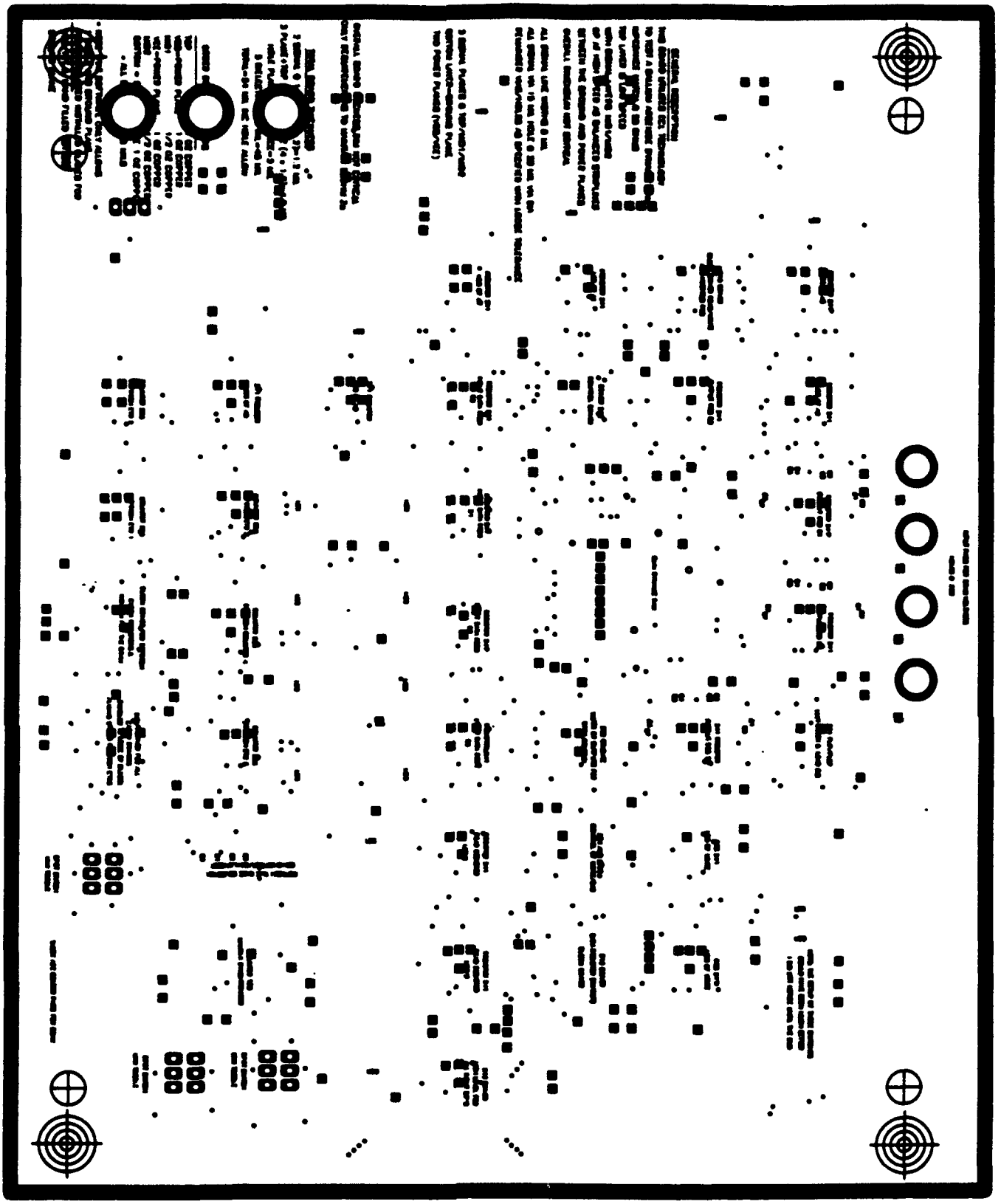


Figure A-1 TOP ASSEMBLY LAYER

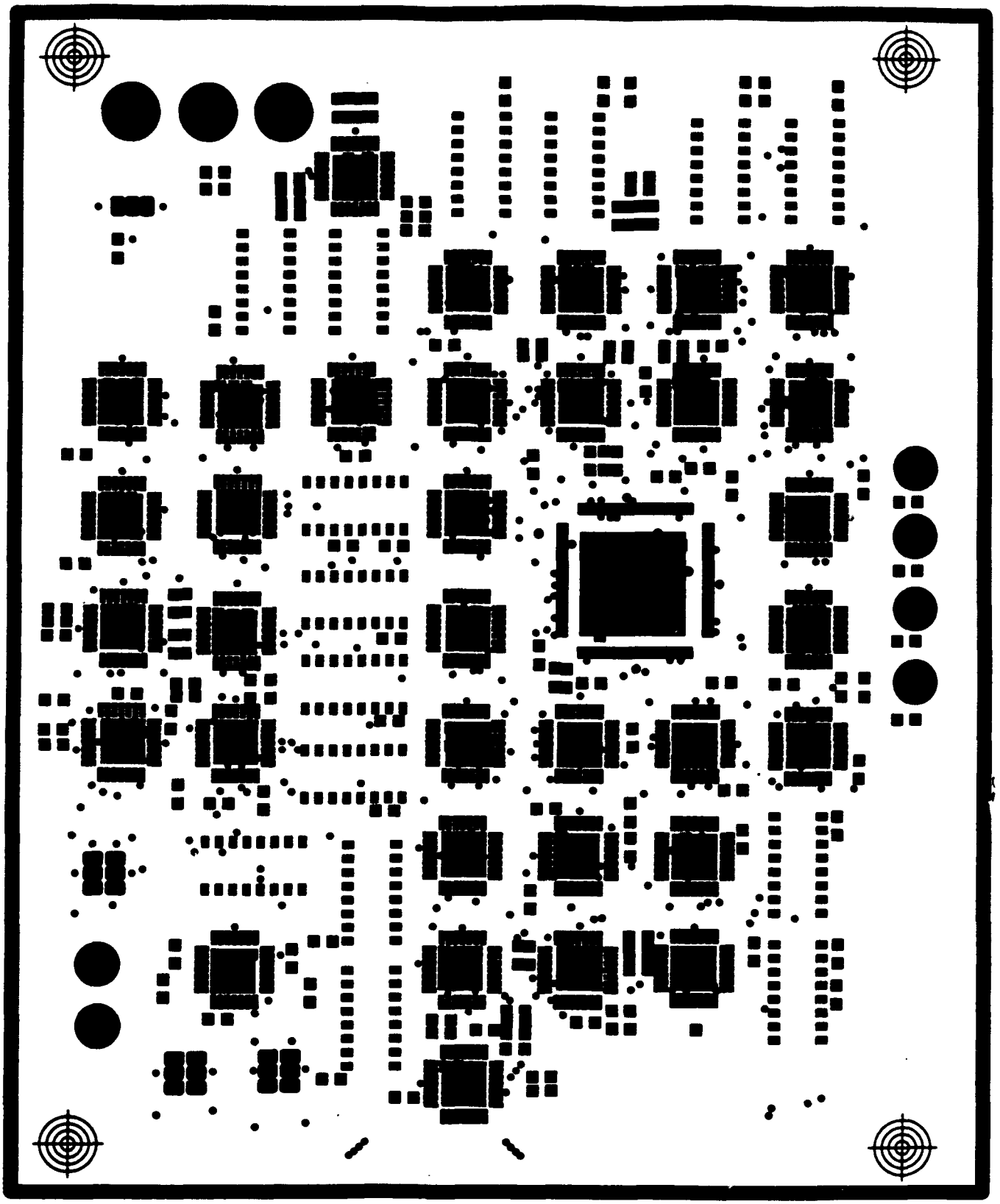


Figure A-2 TOP SOLDER MASK

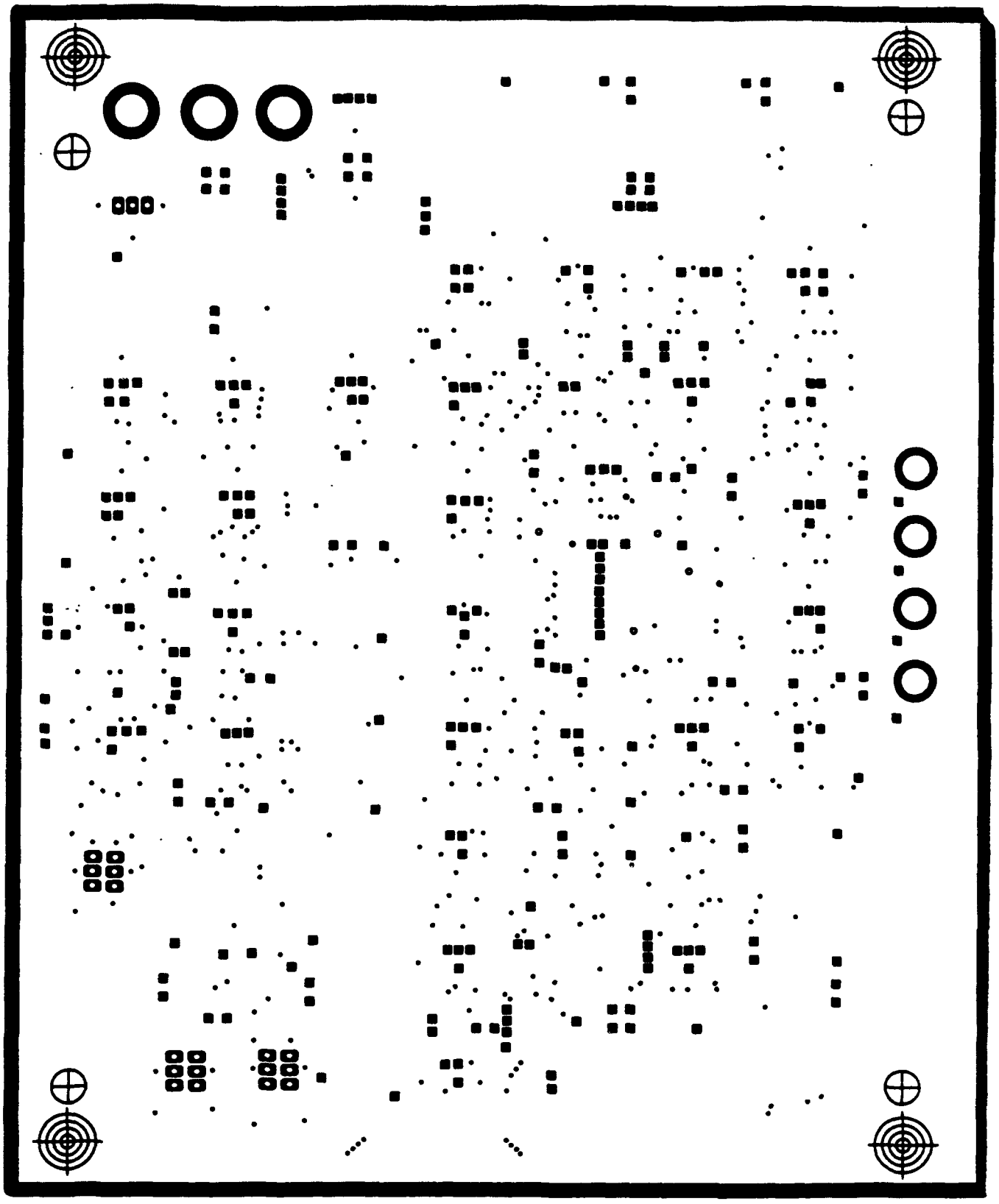


Figure A-3 HOLES AND VIAS PLOT

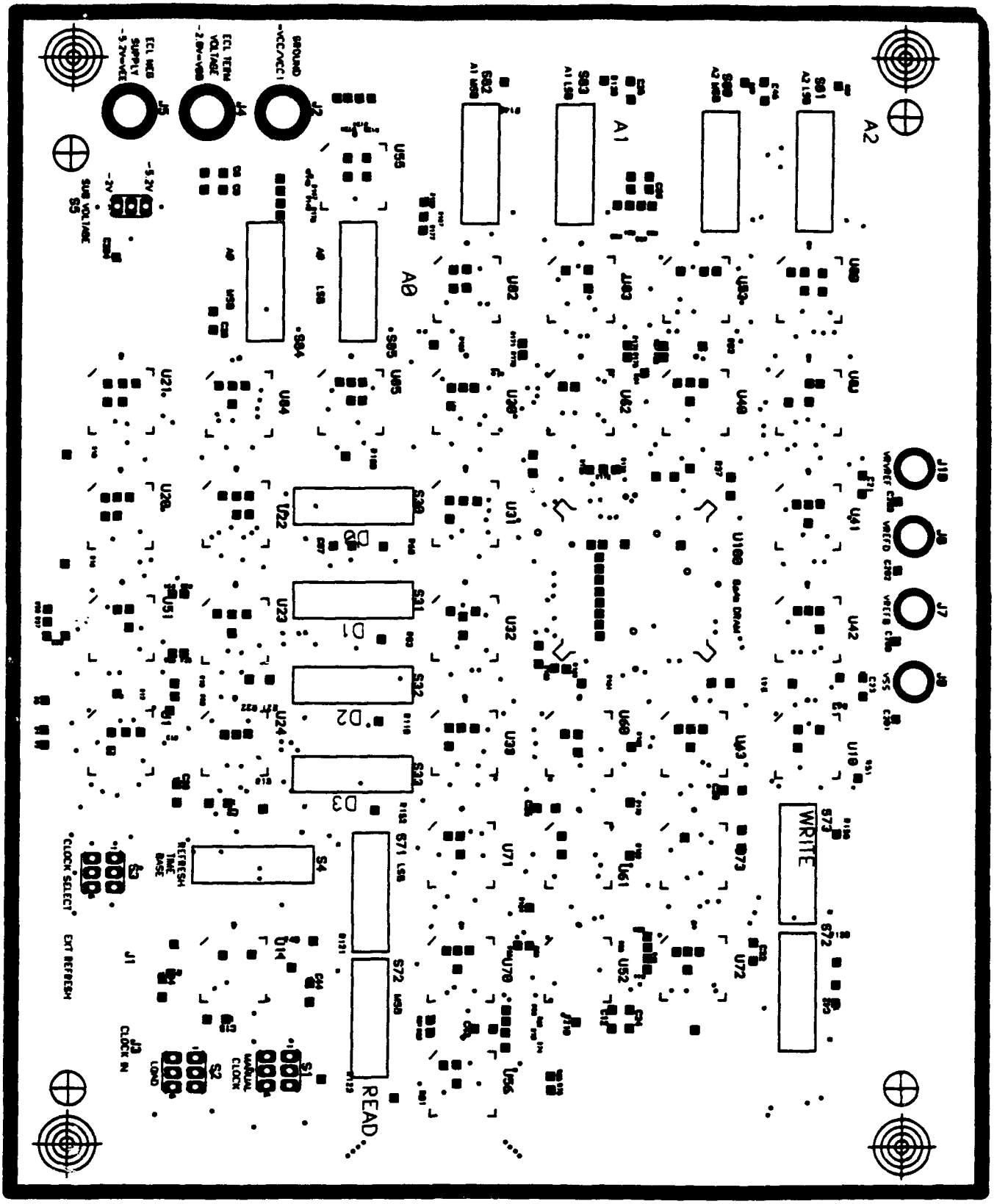


Figure A-4 TOP SILK SCREEN

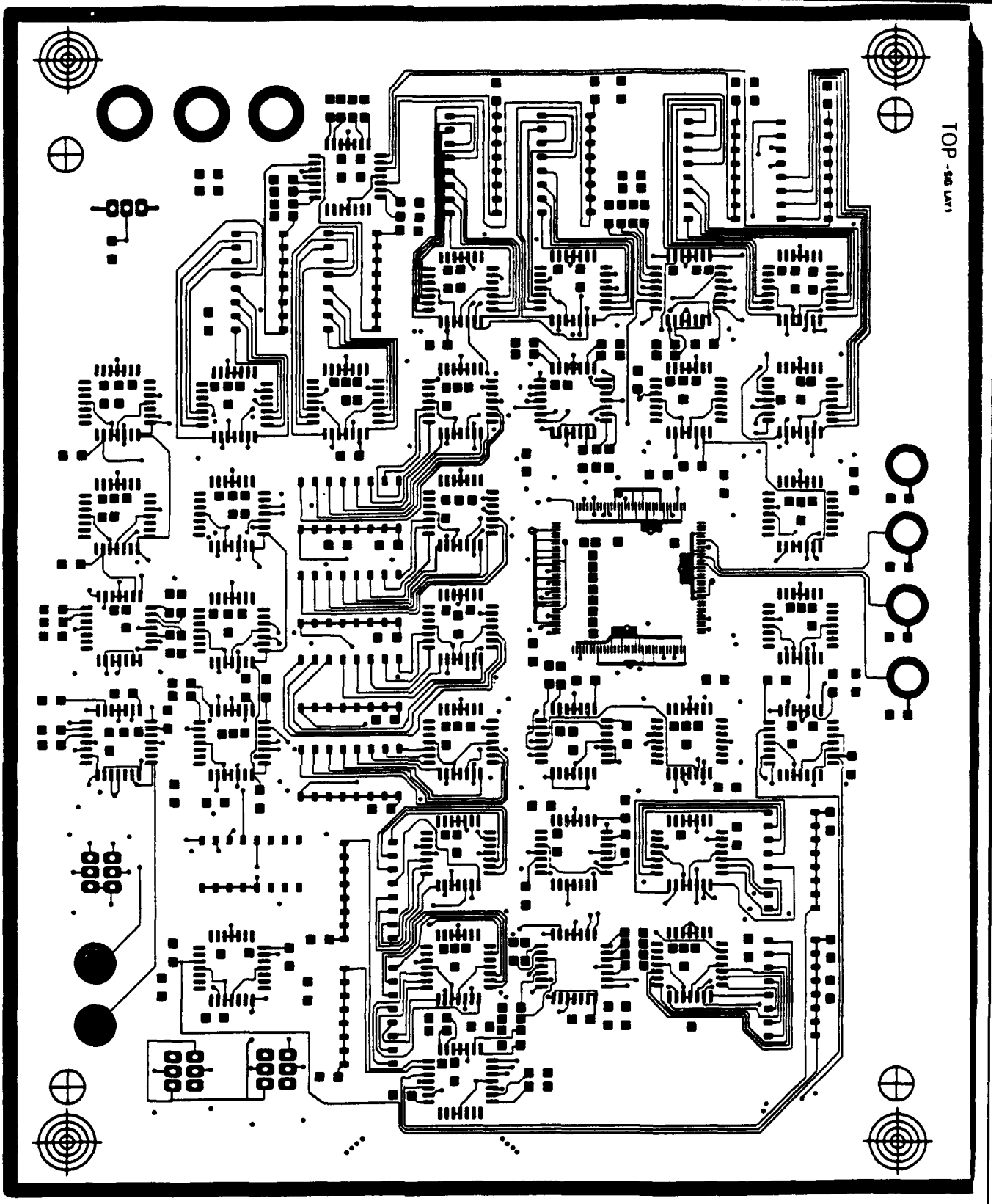


Figure A-5 TOP LAYER PADS AND SLOW SPEED SIGNAL

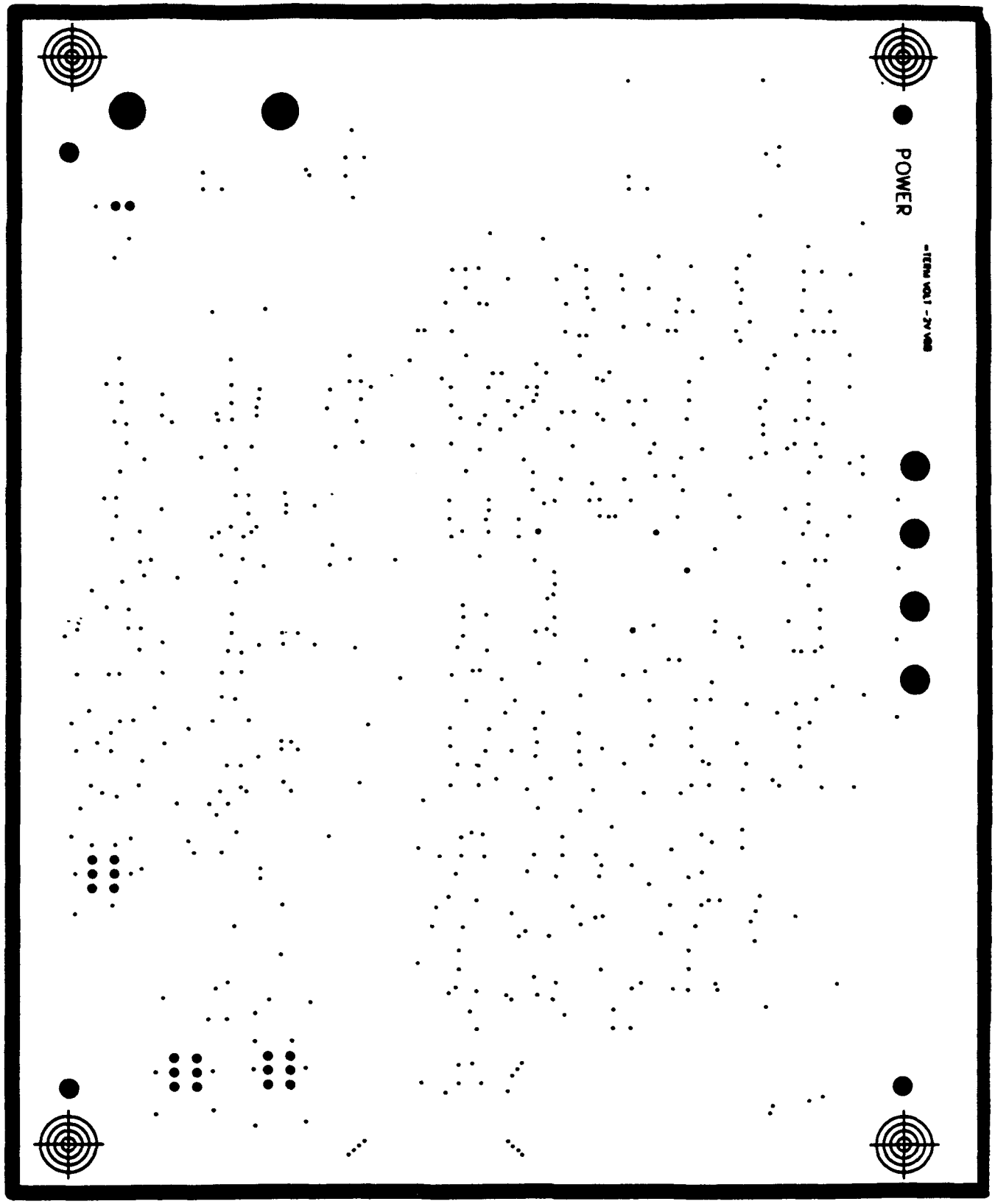


Figure A-6 POWER=VBB TERMINATION LAYER (IN NEGATIVE)

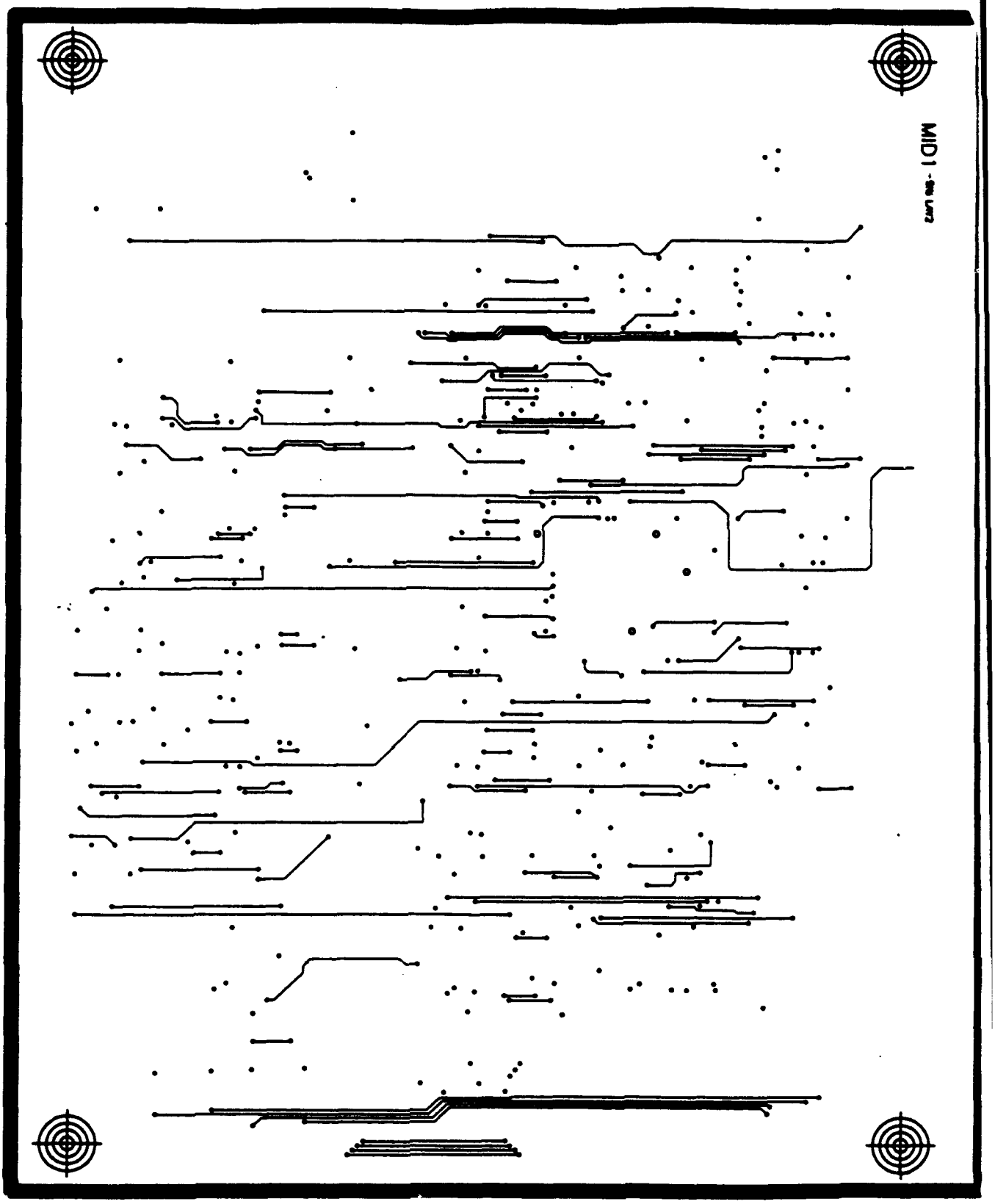


Figure A-7 LAYER MID1=FIRST FAST SIGNAL LAYER

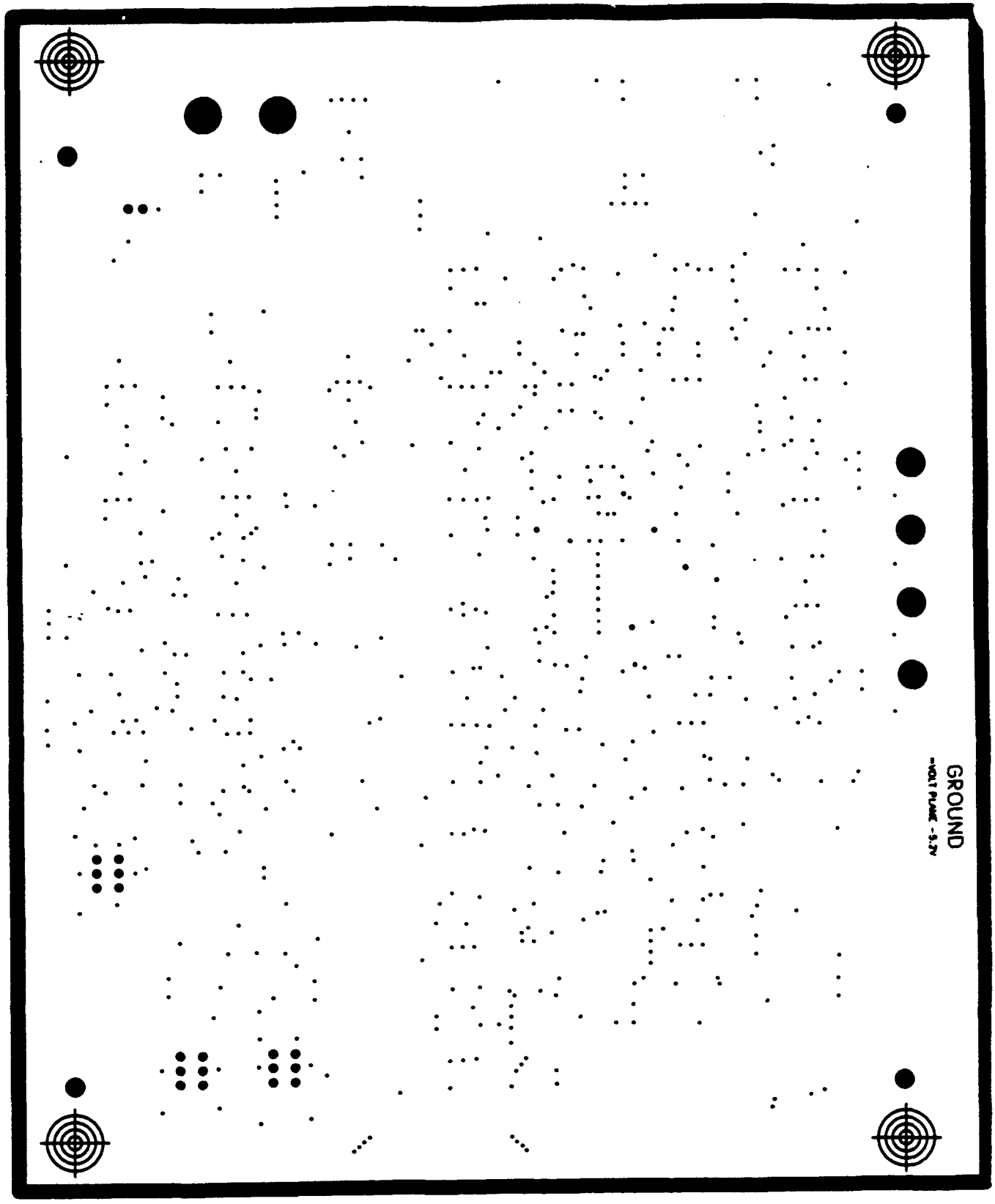


Figure A-8 GROUND=VEE (IN NEGATIVE)

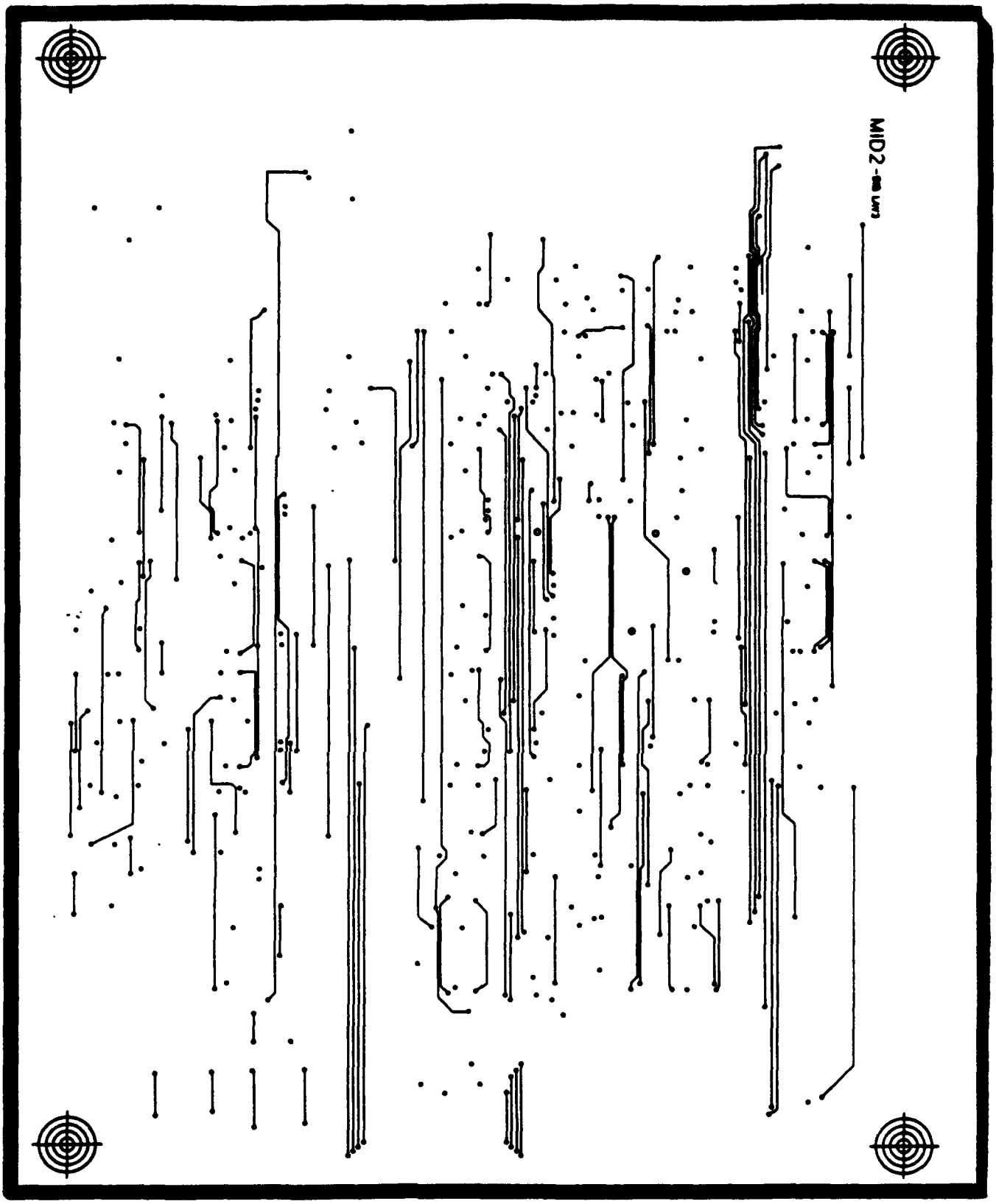


Figure A-9 LAYER MID2=SECOND FAST SIGNAL LAYER

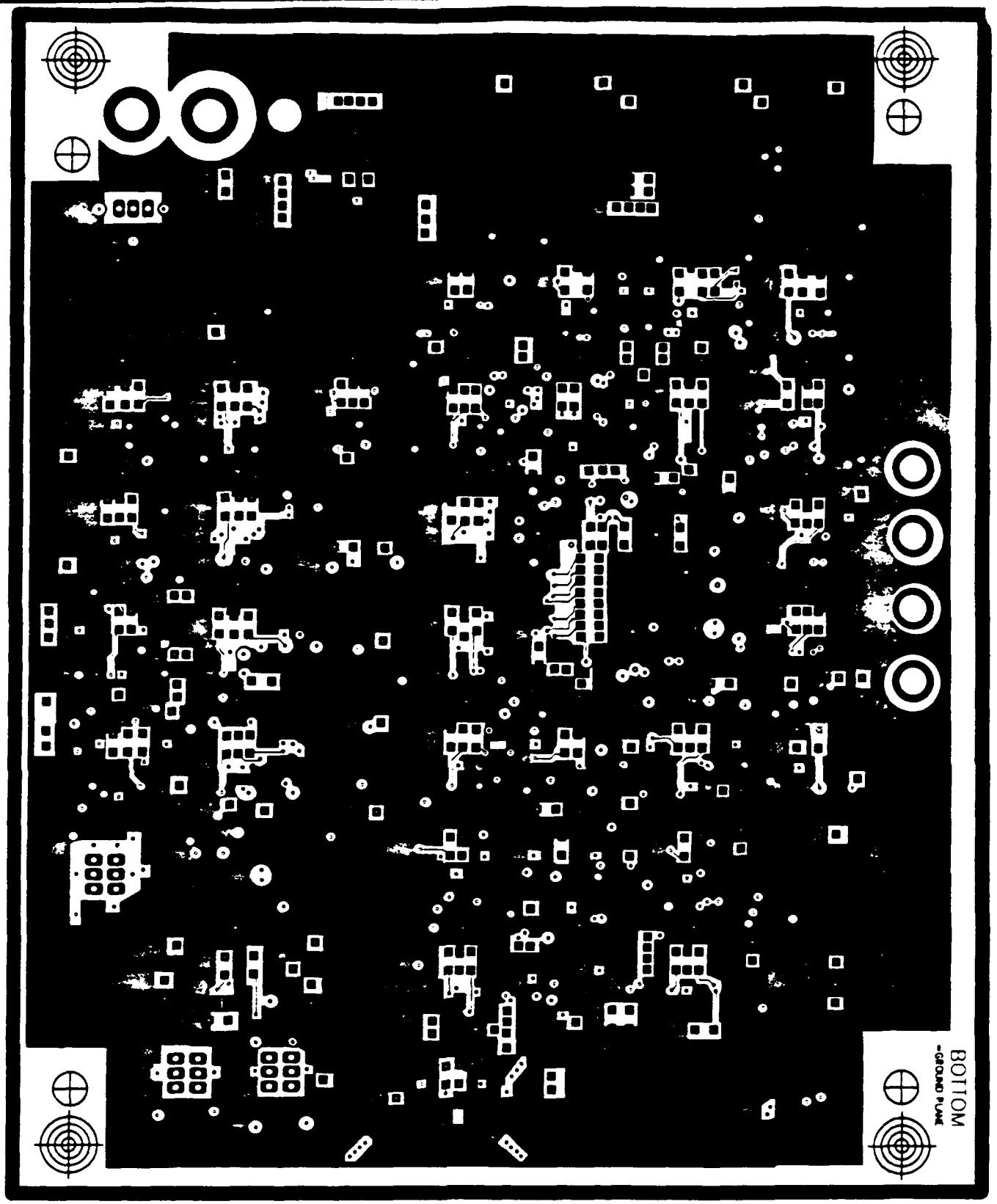


Figure A-10 BOTTOM LAYER=TRUE GROUND PLANE

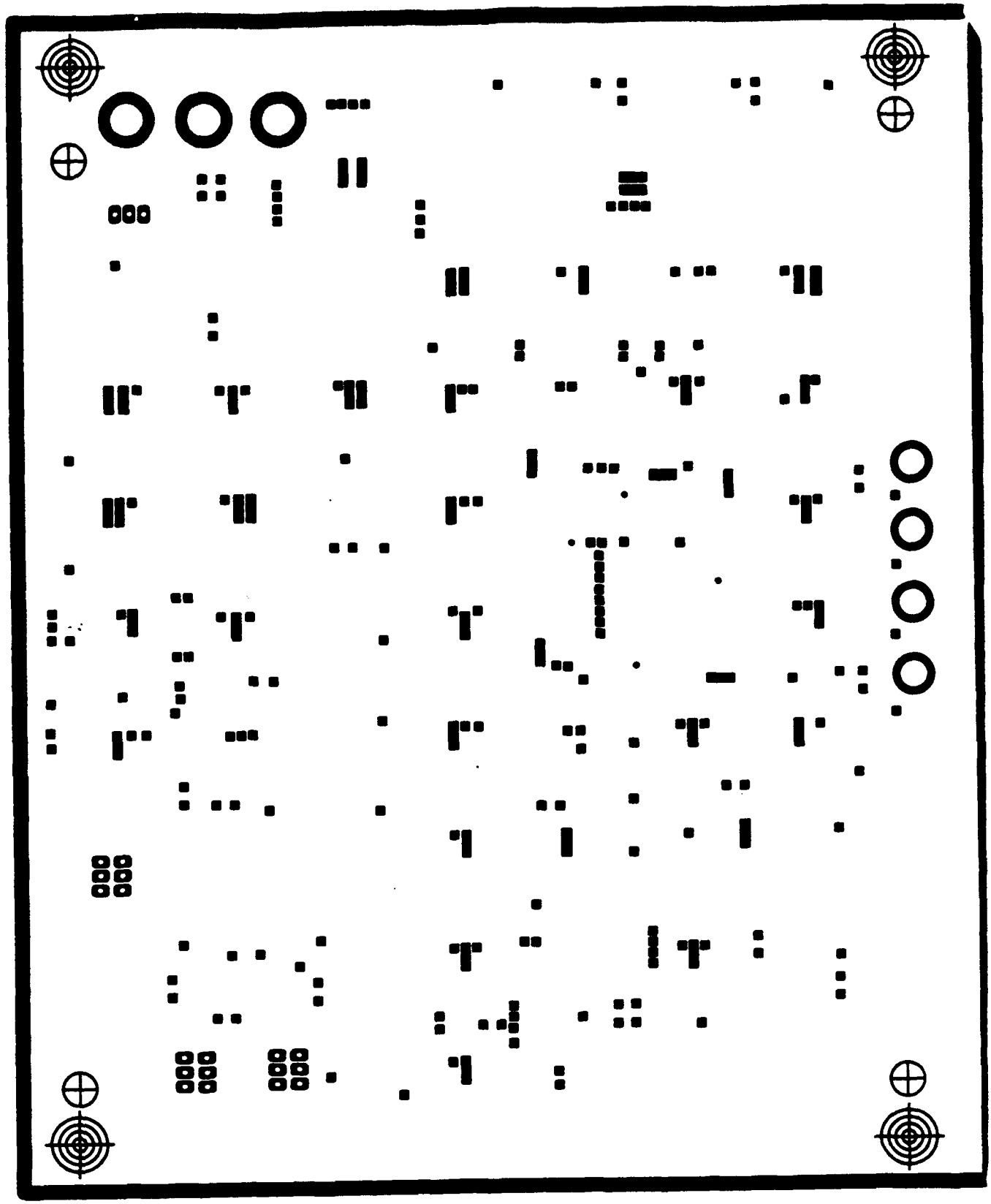


Figure A-11 BOTTOM ASSEMBLY LAYER

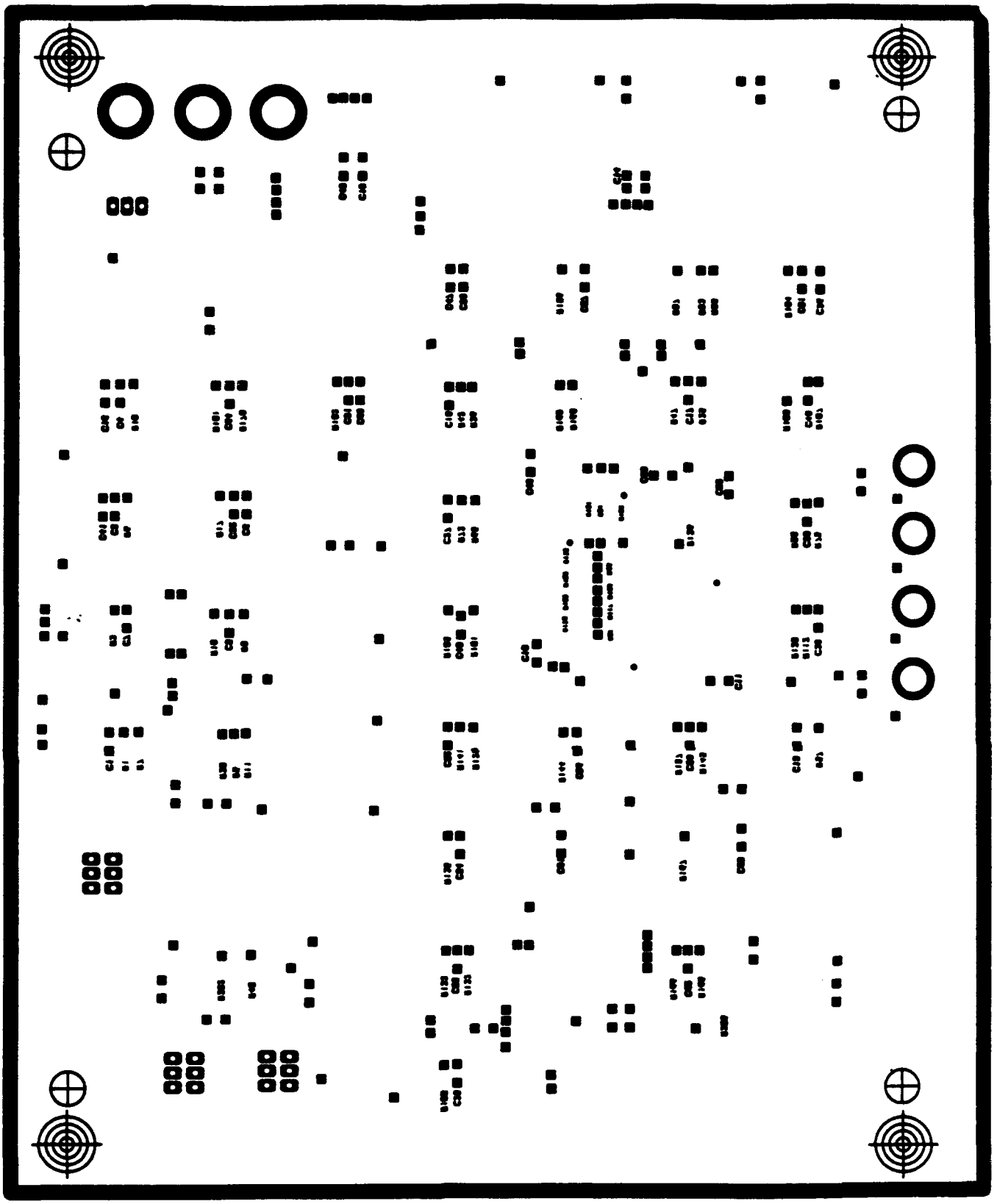


Figure A-12 BOTTOM SILK SCREEN

APPENDIX B

A. APERTURE INFORMATION

Aperture Information COMPLETE.PCB

Aperture and Tool Descriptions

Code	Shape	X	Y	Hole	Type	Comment
D10	Ellipse	008	008	000	Draw	8 Mil Round Draw
D11	Ellipse	010	010	000	Draw	10 Mil Round Draw
D12	Ellipse	012	012	000	Draw	12 Mil Round Draw
D13	Ellipse	020	020	000	Draw	20 Mil Round Draw
D14	Ellipse	050	050	000	Draw	50 Mil Round Draw
D15	Ellipse	030	030	000	Flash	30 Mil Round Flash
D16	Ellipse	040	040	000	Flash	40 Mil Round Flash
D17	Ellipse	050	050	000	Flash	50 Mil Round Flash
D18	Ellipse	060	060	000	Flash	60 Mil Round Flash
D19	Ellipse	070	070	000	Flash	70 Mil Round Flash
D20	Ellipse	100	100	000	Flash	100 Mil Round Flash
D21	Ellipse	110	110	000	Flash	110 Mil Round Flash
D22	Ellipse	200	200	000	Flash	200 Mil Round Flash
D23	Ellipse	210	210	000	Flash	210 Mil Round Flash
D24	Sq Rect	030	030	000	Flash	30 Mil Square Flash
D25	Sq Rect	040	040	000	Flash	40 Mil Square Flash
D26	Sq Rect	050	050	000	Flash	50 Mil Square Flash
D27	Sq Rect	060	060	000	Flash	60 Mil Square Flash
D28	Sq Rect	070	070	000	Flash	70 Mil Square Flash
D29	Sq Rect	100	100	000	Flash	100 Mil Square Flash
D30	Ellipse	100	100	000	Both	Ellipse X_100 Y_100 H_000 FD
D31	Ellipse	032	032	000	Flash	Ellipse X_032 Y_032 H_000 FL
D32	Ellipse	300	300	000	Flash	Ellipse X_300 Y_300 H_000 FL
D33	Ellipse	320	320	000	Flash	Ellipse X_320 Y_320 H_000 FL
D34	Ellipse	400	400	000	Flash	Ellipse X_400 Y_400 H_000 FL
D35	Ellipse	260	260	000	Flash	Ellipse X_260 Y_260 H_000 FL

Code	Shape	X	Y	Hole	Type	Comment
D36	Ellipse	420	420	000	Flash	Ellipse X_420 Y_420 H_000 FL
D37	Ellipse	135	135	000	Flash	Ellipse X_135 Y_135 H_000 FL
D38	Rd Rect	080	120	000	Flash	Rd Rect X_080 Y_120 H_000 FL
D39	Rd Rect	100	140	000	Flash	Rd Rect X_100 Y_140 H_000 FL
D40	Rd Rect	120	080	000	Flash	Rd Rect X_120 Y_080 H_000 FL
D41	Rd Rect	140	100	000	Flash	Rd Rect X_140 Y_100 H_000 FL
D42	Sq Rect	012	060	000	Flash	Sq Rect X_012 Y_060 H_000 FL
D43	Sq Rect	032	080	000	Flash	Sq Rect X_032 Y_080 H_000 FL
D44	Sq Rect	026	080	000	Flash	Sq Rect X_026 Y_080 H_000 FL
D45	Sq Rect	046	100	000	Flash	Sq Rect X_046 Y_100 H_000 FL
D46	Ellipse	025	025	000	Flash	Ellipse X_025 Y_025 H_000 FL
D47	Sq Rect	036	066	000	Flash	Sq Rect X_036 Y_066 H_000 FL
D48	Sq Rect	056	086	000	Flash	Sq Rect X_056 Y_086 H_000 FL
D49	Sq Rect	060	012	000	Flash	Sq Rect X_060 Y_012 H_000 FL
D50	Sq Rect	080	032	000	Flash	Sq Rect X_080 Y_032 H_000 FL
D51	Sq Rect	064	064	000	Flash	Sq Rect X_064 Y_064 H_000 FL
D52	Sq Rect	084	084	000	Flash	Sq Rect X_084 Y_084 H_000 FL
D53	Sq Rect	066	036	000	Flash	Sq Rect X_066 Y_036 H_000 FL
D54	Sq Rect	086	056	000	Flash	Sq Rect X_086 Y_056 H_000 FL
D55	Sq Rect	080	026	000	Flash	Sq Rect X_080 Y_026 H_000 FL
D56	Sq Rect	100	046	000	Flash	Sq Rect X_100 Y_046 H_000 FL
D57	Ellipse	038	038	000	Flash	Ellipse X_038 Y_038 H_000 FL
D70	Sq Rect	110	110	000	Flash	110 Mil Square Flash
D71	Sq Rect	200	200	000	Flash	200 Mil Square Flash
D72	Sq Rect	210	210	000	Flash	210 Mil Square Flash
D73	Target	500	500	000	Flash	500 Mil Target Flash

Code	Hole Diameter
T01	015
T02	020
T03	028
T04	038
T05	060
T06	125
T07	022
T08	050
T09	200
T10	250

B. TOOL ASSIGNMENTS

Aperture and Tool Assignments

Item	Normal	S Mask	Plane	Thermal	Drl Sym	Tool
DRAW APERTURE	D11	-	-	-	-	-
LINE_008	D10	-	-	-	-	-
LINE_010	D11	-	-	-	-	-
LINE_012	D12	-	-	-	-	-
LINE_020	D13	-	-	-	-	-
LINE_100	D30	-	-	-	-	-
P_EL_0040_0040_022_AL	D16	D18	D31	DRAW	-	-
P_EL_0300_0300_000_TL	D32	D33	-	-	-	-
P_EL_0300_0300_200_AL	D32	D33	D23	DRAW	-	-
P_EL_0400_0400_250_AL	D34	D36	D35	DRAW	-	-
P_MH_0250_0250_125_AL	DRAW	-	D37	-	-	-
P_RR_0080_0120_050_AL	D38	D39	D18	DRAW	-	-
P_RR_0120_0080_050_AL	D40	D41	D18	DRAW	-	-
P_SQ_0012_0060_000_TL	D42	D43	-	-	-	-
P_SQ_0026_0080_000_TL	D44	D45	-	-	-	-
P_SQ_0036_0066_000_TL	D47	D48	-	-	-	-
P_SQ_0060_0012_000_TL	D49	D50	-	-	-	-
P_SQ_0064_0064_000_BL	D51	D52	-	-	-	-
P_SQ_0064_0064_000_TL	D51	D52	-	-	-	-
P_SQ_0064_0064_015_AL	D51	D52	D46	DRAW	-	-
P_SQ_0066_0036_000_TL	D53	D54	-	-	-	-
P_SQ_0080_0026_000_TL	D55	D56	-	-	-	-
P_TG_0500_0500_000_AL	D73	-	-	-	-	-
V_CR_030_015	D15	D17	D46	DRAW	-	-
V_CR_050_028	D17	D19	D57	DRAW	-	-
HOLE_015	-	-	-	-	DRAW	T01
HOLE_022	-	-	-	-	DRAW	T07
HOLE_028	-	-	-	-	DRAW	T03
HOLE_050	-	-	-	-	DRAW	T08
HOLE_125	-	-	-	-	DRAW	T06
HOLE_200	-	-	-	-	DRAW	T09
HOLE_250	-	-	-	-	DRAW	T10

- : NOT APPLICABLE. * : APERTURE/TOOL IS NOT ASSIGNED.

C. BILL OF MATERIALS

Bill of Materials — COMPLETE.PCB

Quantity	Type	Value	Ref Designators
1	100302-PCC		U60
1	100302-PCC		U1
1	100304-PCC		U61
1	100313-PCC		U62
5	100313-PCC		U51,U52,U53,U55,U56
1	100331-PCC		U10
4	100336-PCC		U21,U22,U23,U24
2	100336-PCC		U11,U20
17	100341-PCC		U31,U32,U33,U40,U41,U42, U43,U70,U71,U72,U73,U80, U81,U82,U83,U84,U85
1	100341-PCC		U30
1	BAN-IN	CLOCK	J3
1	BAN-IN	GND	J2
1	BAN-IN	REFRESH	J1
1	BAN-IN	VBB	J4
1	BAN-IN	VEE	J5
1	BAN-IN	VREFB	J7
1	BAN-IN	VREFD	J8
1	BAN-IN	VRVREF	J10
1	BAN-IN	VSS	J9
69	CAP-SM	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16,C17,C18,C19,C20, C21,C22,C23,C24,C25,C26, C27,C28,C29,C30,C31,C32, C33,C34,C35,C36,C37,C38, C39,C40,C41,C42,C43,C44, C45,C46,C47,C48,C49,C50, C51,C52,C53,C54,C55,C56, C57,C58,C59,C60,C61,C62, C63,C64,C200,C201,C202, C203,C204	
1	GAASD	U100	
3	SW-DPDT	S1,S2,S3	

NOTE: BAN-IN is a .25 inch jack plug for power supplies. May be supplemented by a 1/4 inch bolt to run power onto board.

15	SW-THDIPSM	S4,S30,S31,S32,S33,S70, S71,S72,S73,S80,S81,S82, S83,S84,S85	NOTE: These are the 8 position DIP
1	SWITCHSPDT	S5	
137	TERMX	R2,R4,R5,R6,R8,R9,R10,R11, R12,R13,R15,R16,R17,R18, R19,R20,R21,R22,R29,R30, R35,R36,R37,R38,R39,R40, R41,R42,R44,R46,R47,R49, R53,R55,R58,R59,R60,R62, R64,R65,R66,R67,R68,R70, R72,R74,R75,R78,R80,R81, R83,R84,R86,R87,R88,R89, R90,R91,R92,R93,R94,R95, R96,R97,R98,R99,R100,R101, R102,R103,R104,R105,R106, R107,R108,R109,R112,R117, R119,R120,R121,R123,R124, R125,R126,R127,R128,R129, R149,R153,R155,R156,R157, R159,R160,R161,R162,R163, R165,R166,R167,R168,R169, R170,R171,R172,R173,R174, R175,R176,R177,R178,R179, R180,R181,R182,R183,R184, R185,R202,R205,R210	
12	TERMX	R1,R3,R7,R23,R24,R25,R27, R28,R51,R57,R63,R158	
1	TERMX	R26	

D. LIBRARY CONTENTS

Library Contents BUTLERSM.LIB

Total Patterns: 9

BANANNA	CC1206	CTSDIP8	DPDTTOG
PLCC28A	PLCC132M	QFP100A	RC1206
SPDT-TOG			

Library Contents PCBSMT.LIB

Total Patterns: 114

CC0805	CC1206	CC1210	CC1812
CC1825	DPAK	DPAK(A1A2K)	DPAK(BEC)
MELF1/4W	MLL34	MLL41	MO-003/10
MO-003/14	MO-004/10	MO-004/14	MO-004/16
MO-018/40	MO-019/24	MO-019/28	MO-020/36
MO-020/40	MO-021/16	MO-021/24	MO-021/36
MO-022/20	MO-022/42	MO-023/36	MO-023/50
PLCC18RJ	PLCC18RJL	PLCC20J	PLCC22RJ
PLCC28A	PLCC28J	PLCC28RJ	PLCC32RJ
PLCC44A	PLCC44J	PLCC52A	PLCC52J
PLCC68	PLCC68A	PLCC68J	PLCC84J
PLCC84M	PLCC100J	PLCC100M	PLCC124J
PLCC132M	PLCC164M	PLCC196M	PLCC244M
QFP44	QFP48	QFP52	QFP54
QFP64	QFP70	QFP80	QFP100
QFP100A	RC0805	RC1206	RC1210
SO8	SO14	SO16	SOD80
SOJ14	SOJ16	SOJ18	SOJ20
SOJ22	SOJ24	SOJ26	SOJ28
SOL14	SOL16	SOL20	SOL24
SOL28	SOT89	SOT-23	SOT-23(A1A2K)
SOT-23(AK1K2)	SOT-23(AKK/A)	SOT-23(ANK)	SOT-23(BEC)
SOT-23(DSG)	SOT-23(EBC)	SOT-23(GKA)	SOT-23(GSD)
SOT-23(K1K2A)	SOT-23(KAG)	SOT-23(KAK/A)	SOT-23(KGA)
SOT-23(NAK)	SOT-23(NKA)	SOT-23(SDG)	SOT-89
SOT-89(BCE)	SOT-143	SOT-143(CE1E2B)	S OT-143(OG)
TC3216	TC3518	TC3527	TC3528

E. PCB STATISTICS

PCB Statistics PCBSMT.LIB

Arcs: 327 Components: 282 Pads: 1804 Polygons: 602
Lines: 6016 Text strings: 820 Vias: 464 Holes: 783

Text Summary -

T_0028_008_0:	176
T_0028_008_1:	15
T_0028_008_3:	13
T_0028_008_4:	11
T_0040_008_0:	88
T_0040_008_1:	16
T_0040_008_2:	26
T_0040_008_3:	45
T_0040_008_4:	108
T_0040_008_5:	1
T_0040_008_6:	5
T_0040_008_7:	8
T_0040_010_0:	22
T_0040_010_1:	2
T_0040_010_2:	7
T_0040_010_3:	14
T_0040_010_4:	72
T_0040_010_5:	3
T_0040_010_6:	3
T_0048_008_0:	45
T_0060_010_0:	92
T_0060_010_1:	3
T_0060_010_2:	4
T_0060_010_3:	8
T_0060_012_0:	18
T_0100_008_0:	11
T_0100_008_3:	4

Line Summary -
L_008: 5090
L_010: 644
L_012: 492
L_020: 113
L_100: 4

Pad Summary -
P_EL_0040_0040_022_AL: 4
P_EL_0300_0300_000_TL: 2
P_EL_0300_0300_200_AL: 4
P_EL_0400_0400_250_AL: 3
P_MH_0250_0250_125_AL: 4
P_RR_0080_0120_050_AL: 18
P_RR_0120_0080_050_AL: 3
P_SQ_0012_0060_000_TL: 66
P_SQ_0026_0080_000_TL: 476
P_SQ_0036_0066_000_TL: 160
P_SQ_0060_0012_000_TL: 66
P_SQ_0064_0064_000_BL: 63
P_SQ_0064_0064_000_TL: 92
P_SQ_0064_0064_015_AL: 283
P_SQ_0066_0036_000_TL: 80
P_SQ_0080_0026_000_TL: 476
P_TG_0500_0500_000_AL: 4

Via Summary -
V_CR_030_015: 460
V_CR_050_028: 4

Hole Summary -
H_015: 743
H_022: 4
H_028: 4
H_050: 21
H_125: 4
H_200: 4
H_250: 3

Plane Connections -
Power Thermals: 0
Power Directs: 186
Ground Thermals: 0
Ground Directs: 100

F. DESIGN RULE CHECK

Design Rule Check Report PCBSMT.LIB

==========

DRC Clearances (in mils)

	Top	Bot	Mid1	Mid2	Mid3	Mid4	Mid5	Mid6	Mid7	Mid8
Pad-to-Pad	10	10	10	10	10	10	10	10	10	10
Pad-to-Line	10	10	10	10	10	10	10	10	10	10
Line-to-Line	10	10	10	10	10	10	10	10	10	10

Hole-to-Hole 30

DRC Report Options

Clearance Violations:	enabled
Text Violations:	disabled
Net List Violations:	enabled
Single Node Routes:	enabled
Unconnected Pins:	disabled
Unplaced Nodes:	disabled

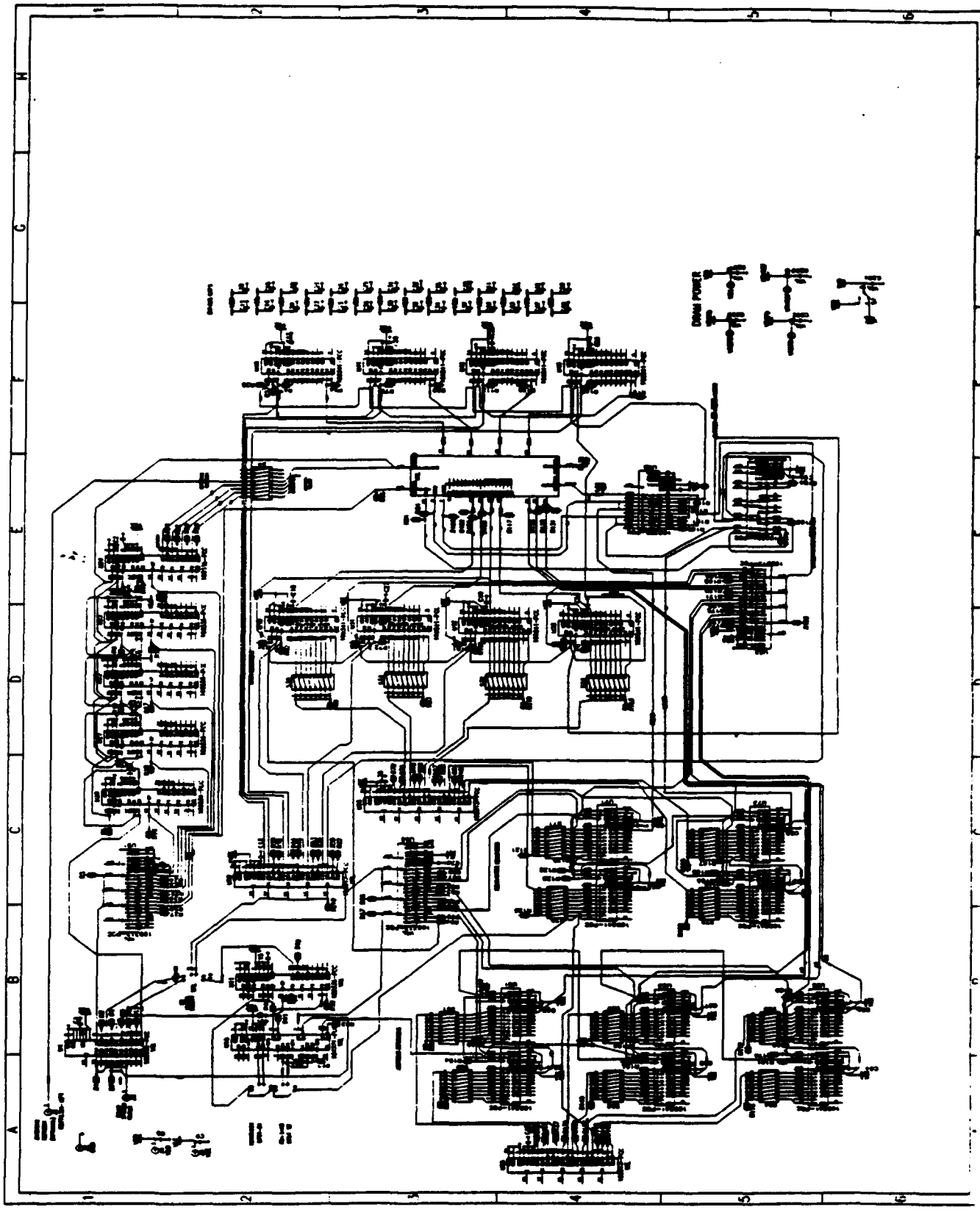
DRC Errors

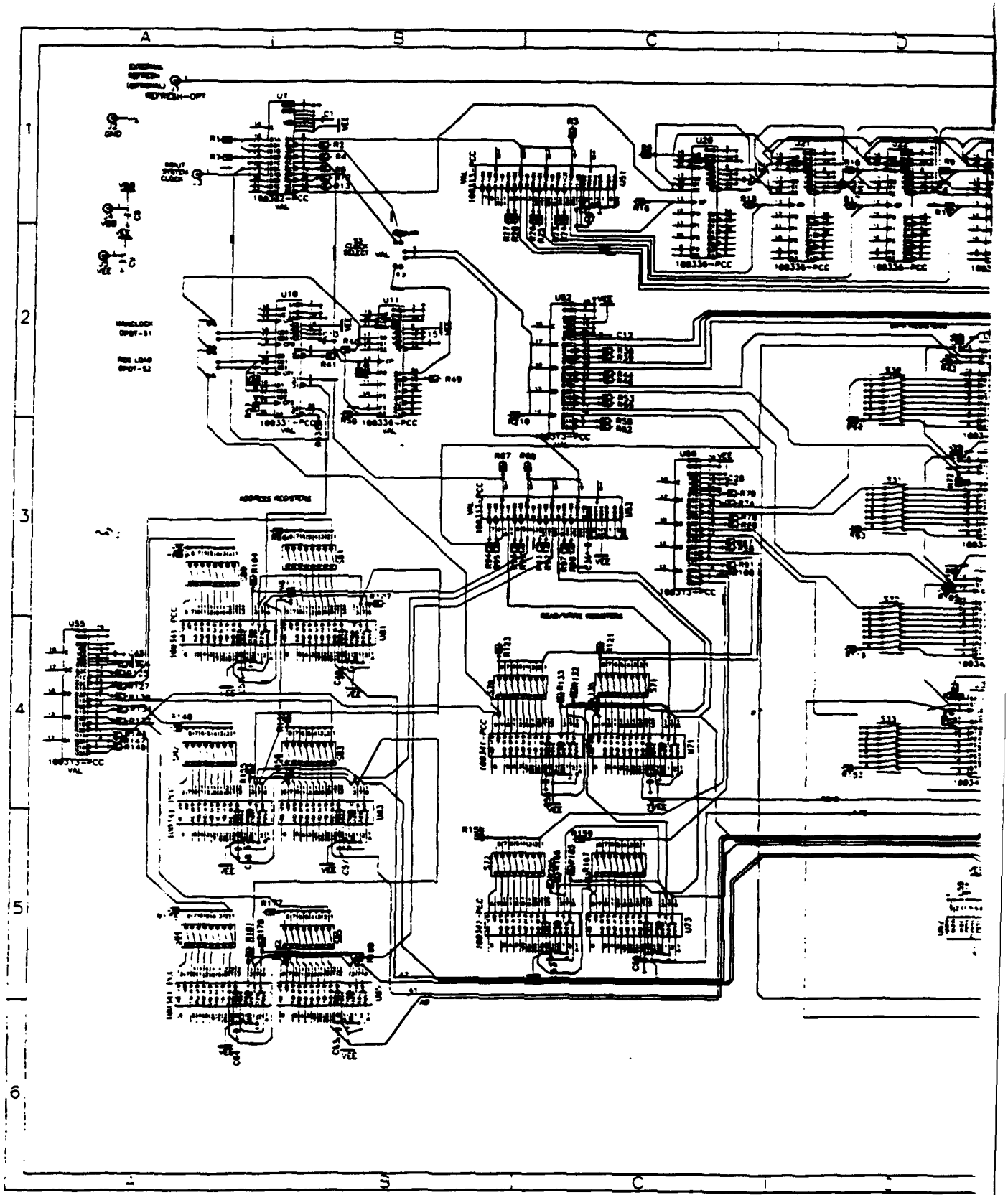
DRC Summary

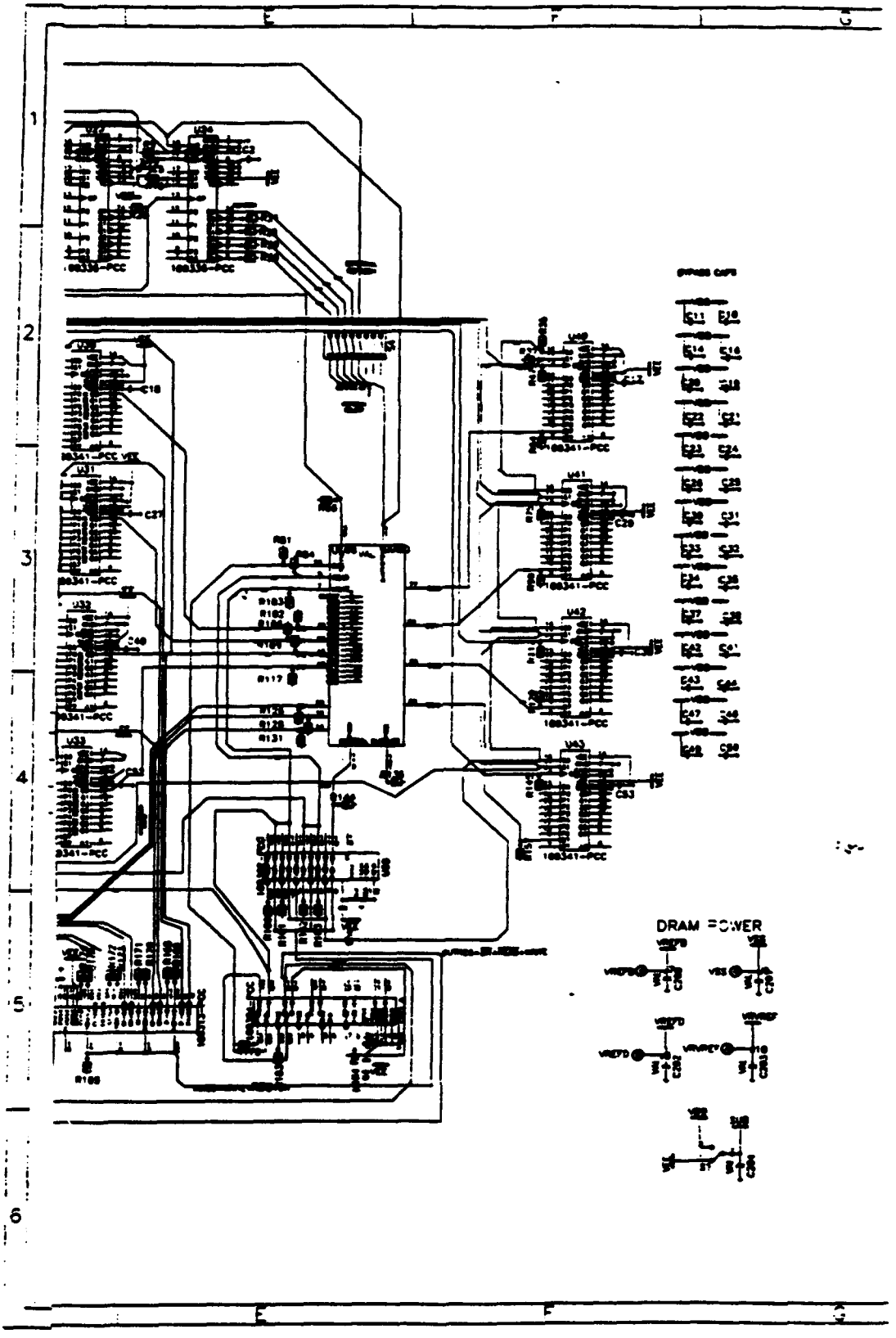
0 errors detected

APPENDIX C

This Appendix contain the schematic prints from TANGO Schematic. The first is an overall print and the following are enlarged views. For reference, the numbering convention of parts is not standard. This was done to enable the easiest placement of the components in the PCB program as it keys on the number for placement. To have some control over the placement operation the operational groups were given their own number sequence (ie. Refresh (2X), Data Registers (3X), Output Registers (4X), etc.).






DRAM POWER

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